Chapter-I

(The Processor 8086/8088- Architecture, Pin Diagrams & Timing Diagram)

Short type questions [2 marks each]

Q-1) **What is the function of lock signal?[S-16(Q1-a)]**

Ans:- Lock signal indicates that other system bus masters will be prevented from gaining the system bus, while this signal is low. When this signal is activated, it ensures that other processors connected in the system will not gain the control bus when the CPU is executing a critical instruction which requires the system bus.

Q-2) **What are various segment registers in 8086 and name them? [S-17(Q1-a)]**

Ans:- The 8086 μP four segment registers. They are-

- ♣ Code Segment Register (CS)
- ♣ Data Segment Register (DS)
- ♣ Extra Segment Register (ES)
- ♣ Stack Segment Register (SS)

Q-3) **What is minimum mode of 8086 system? [S-17(Q2-a)]**

Ans:- In minimum mode, all the control signals are given out by the μP chip itself. There is a single μP in the minimum mode system. The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices.

Q-4)**Name the interrupts of 8086. [W-17(Q1-a)]**

Ans:- The interrupts of 8086μP are NMI, TRAP, Divide by zero interrupt, Overflow interrupt, etc.

Q-5)**What is $\overline{\text{DEN}}$. [S-19(Q1-a)]**

Ans:- Data Enable. This signal indicates the availability of valid data over the address/data line. It is used to enable the transreceivers to separate the data from the multiplexed address/data signal.

Q-6) **What happened when processor executes a HLT instruction? [S-19(Q2-a)]**

Ans:- When the processor executes a HLT instruction, it enters the 'halt' state.

Q-7) **Write down two comparison between 8086 and 8088 [S-19(Q3-a)]**

Ans:-

The two comparison between 8086 & 8088 are-

1) The predecoded code queue length is 4-bytes in 8088 while it is 6-bytes in 8086.
2) The 8088 BIU will fetch a byte from the memory to load the queue each time if 1-byte is free. In 8086, at least 2-bytes should be free for the next fetch operation.

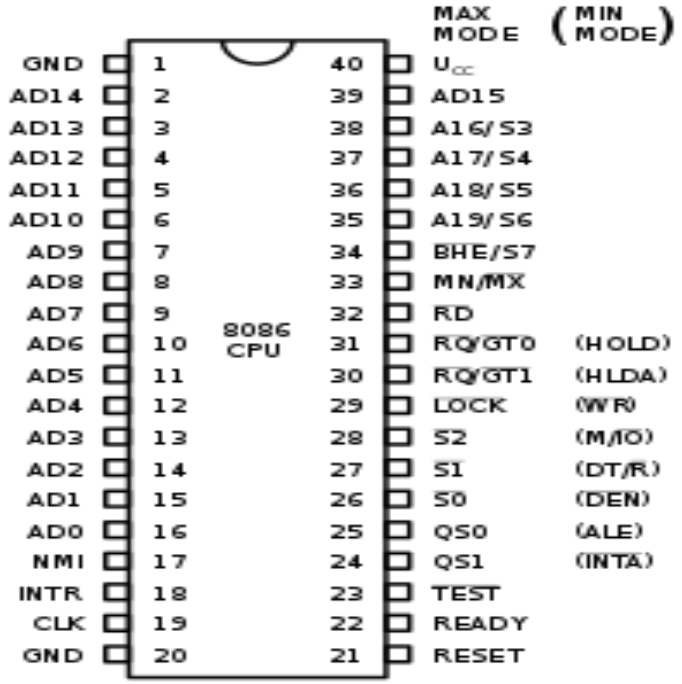
Medium type questions [5 marks each]

Q-1) **Draw the pin configuration of 8086 and explain briefly function of each pin. [S-16(Q1-b)], [S-17(Q1-c)], [W-17(Q1-c)]**

Ans:-The 8086 μP is 16-bit CPU packaged in a 40 pin CERDIP or plastic package. Some of the pin serves a particular function in minimum mode and others function in maximum mode.

The signals can be categorised in three groups-

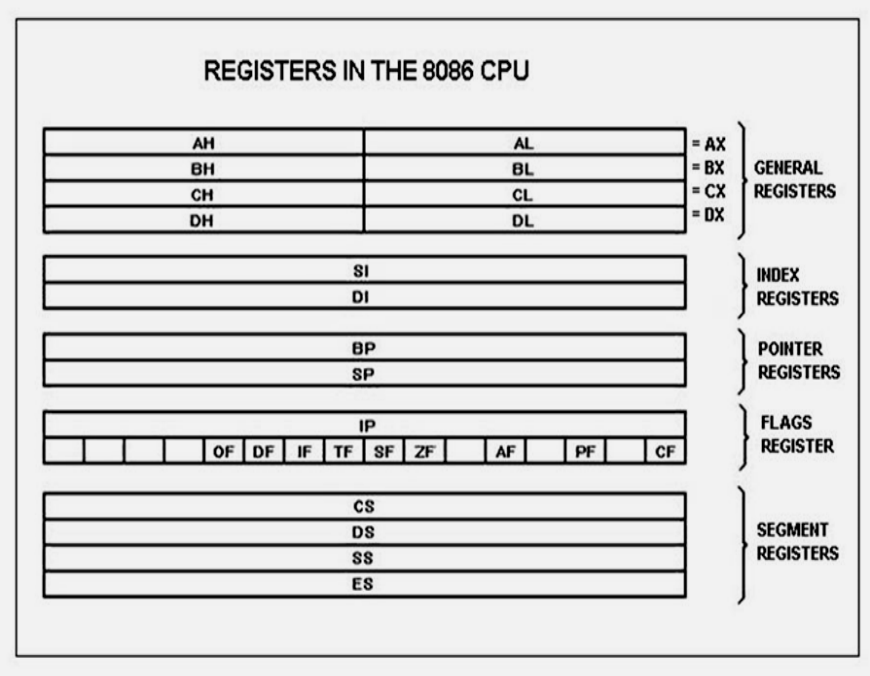
i. Signals having common function in MN & MX mode.
ii. Functions in only minimum mode.
iii. Functions in only maximum mode.



- ***AD_{15} – AD_0(Pin 2-16)-*** These are time multiplexed memory I/O address & data lines. Address remains on during T1 state and data on the data bus during T_2, T_3, T_w and T_4. These lines are active high and float to a tri-state during interrupt acknowledge and local bus hold acknowledge cycles.
- ***A_{19}/S_6 ,A_{18}/S_5, A_{17}/S_4, A_{16}/S_3-*** These are time multiplexed address & status lines. During T_1, these are most significant address lines for memory operations. During I/O operation, these lines are low. The status line S_6 always low.
- ***$\overline{BHE}/S_7$*** – Bus High Enable/Status. The BHE is used to indicate the transfer of data over the higher order (D_{15}-D_8)data bus.
- ***$\overline{RD}$***– Read signal, when low, indicates the peripherals that processor is performing a memory or I/O read operation.
- ***READY***– This is the acknowledgement from the slow devices or memory that has completed the data transfer.
- ***INTR***– Interrupt request is a level triggered i/p. If any interrupt request is pending, the process or enters into INTA cycle.
- ***TEST***– This i/p is examined by a 'WAIT' instruction. If it goes low, execution will continue, else, the processor remains in an idle state.
- ***NMI***– This is Non maskable interrupt. A transaction from low to high initiates the interrupt response at the end of the current instruction.
- ***RESET***– It terminates the current activity and start execution from FFFF0 H.
- ***CLK***– Clock i/p provides the basic timing for processor operation and bus control activity.

- ***VCC***– +5 Volt power supply for operation of internal ckt.
- ***GND***– Ground for internal ckt.
- ***MN/$\overline{MX}$***– The logic level at this pin decides whether the processor is to operate in either minimum or maximum mode.

Q-2) **Explain register organisations of 8086.[S-17(Q1-b)], [S-19(Q1-c)]**
Ans:-

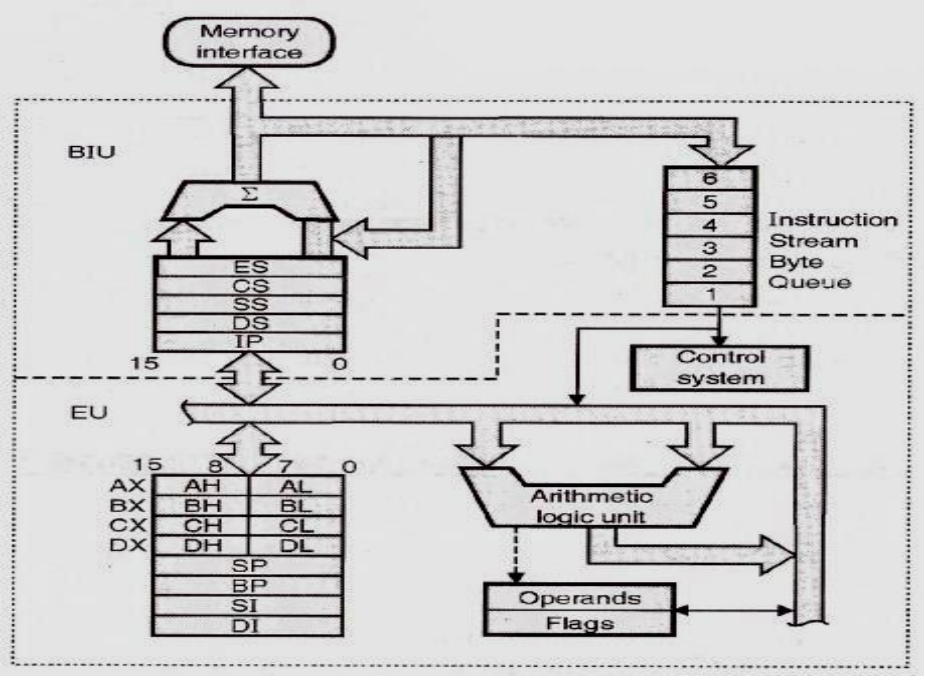


The 8086 μP has a powerful set of 16-bit registers known as GPR and SPR. These are categorized in 4 groups-

- *General Data Registers*- The registers AX, BX, CX and DX are the GPR. AX is used as 16-bit accumulator as AL & AH. AL can be used as 8-bit accumulator for 8-bit operation. DX may be used as an implicit operand or destination in case of few instructions. All registers are used for holding data, variables and immediate results temporarily.
- *Segment Registers*- There are four segment registers as CS, DS, ES and SS. The CS is used for addressing a memory location in the code segment of memory, where the program is stored. The DS register points to the data segment of the memory, where the data is resided. The ES register also refers to a segment which essentially is another data segment of memory. The SS register is used for addressing stack segment of memory.
- *Pointers and Index Registers*–The pointers contain the offset within the particular segments. The pointers IP, BP and SP usually contain the offsets within the code and stack segment. The index registers are used as GPR as well as for offset storage in case of indexed, based indexed and relative based indexed addressing modes. The register SI is generally used to store the offset of source data in data segment while the register DI is used to store the offset of destination in data or extra segment.
- *FLAG/PSW Register*–The content of the flag register/PSW indicates the results of computations in the ALU. It also contains some flag bit to control the CPU operation.

Q-3)**Draw the architecture of 8086 with proper description. [W-17(Q1-b)], [S-19(Q7-c)]**

Ans:- The 8086 μP supports a 16-bit ALU, a set of 16-bit registers & segmented memory addressing capability, a rich instruction set, powerful interrupt structure, fetched instruction queue & execution etc. The internal block diagram is shown below--



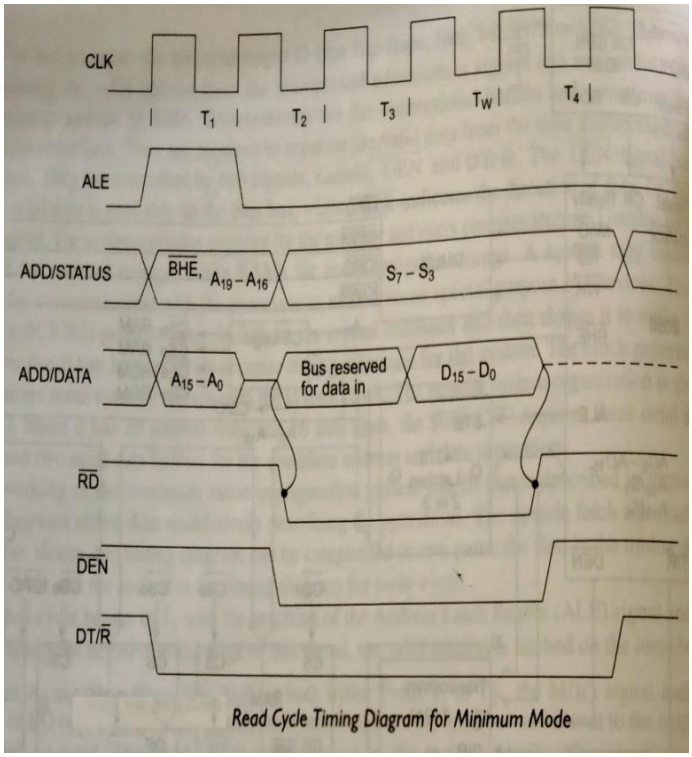
The complete architecture of 8086μP can be divided into two parts- (a) Bus Interface unit(BIU) and (b)Execution unit(EU)

The BIU contains the circuit for physical address calculation and a predecoding instruction queue(6byte long). It makes the system's bus signals available for external interfacing of the devices. The complete 20-bit physical address is generated using segment and offset register. The content of a segment register also called as segment address is shifted left bit-wise four times and to this result, content of an offset register also called as offset address is added, to produce physical address. The segment register indicates the base address of a particular segment and offset indicates the distance of the required memory location in the segment from the base address. The BIU has a separate adder to perform the operation of obtaining physical address. The segment address is to be taken from the CS, DS, SS or ES, while the offset may be the content of IP, BX, SI, DI, SP, BP or an immediate 16-bit value. While the fetched instruction is executed internally, the external bus is used to fetch the machine code of the next instruction and arrange it in a queue known as predecoded instruction byte queue of 6-bytes long FIFO structure. The instruction from the queue are taken for decoding sequentially, once a byte is decoded, the queue is rearranged by pushing it out and fetch the next opcode.

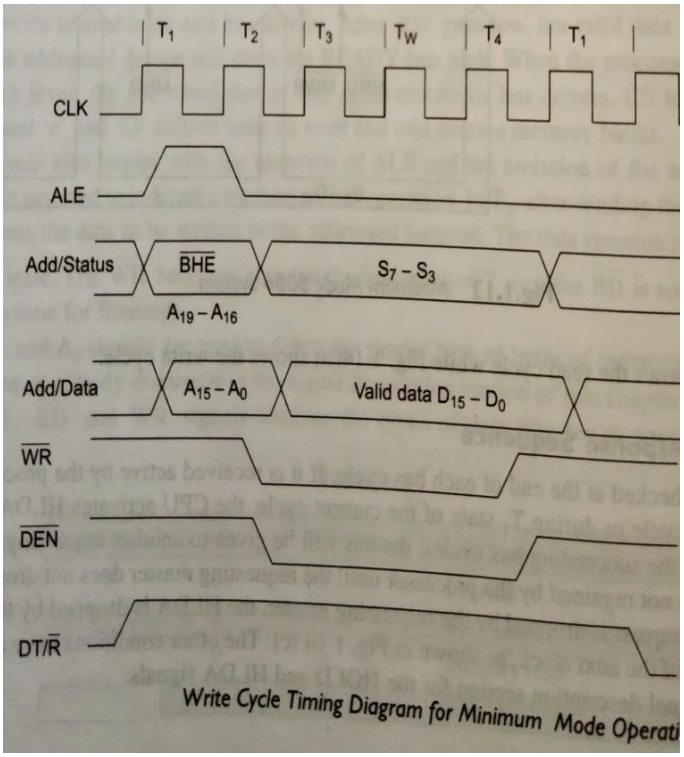
While the opcode is fetched by the BIU, the EU executes the previously decoded instruction concurrently. The BIU along with the EU forms a pipeline. The EU contains the register set of 8086 except segment registers & IP. It has a 16-bit ALU, able to perform arithmetic and logic operations. The 16-bit flag register reflects the results of execution by the ALU. The decoding unit decodes the opcode bytes issued from the instruction byte queue. The timing and control unit drives the necessary control signals to execute the instruction opcode received from the queue. The EU may pass the result to the BIU for storing them in memory.

Q-4) **Draw the read and write timing diagram for minimum mode. [S-19(Q1-b)]**

Ans:-



Read Cycle Timing Diagram for Minimum Mode



Write Cycle Timing Diagram for Minimum Mode Operati

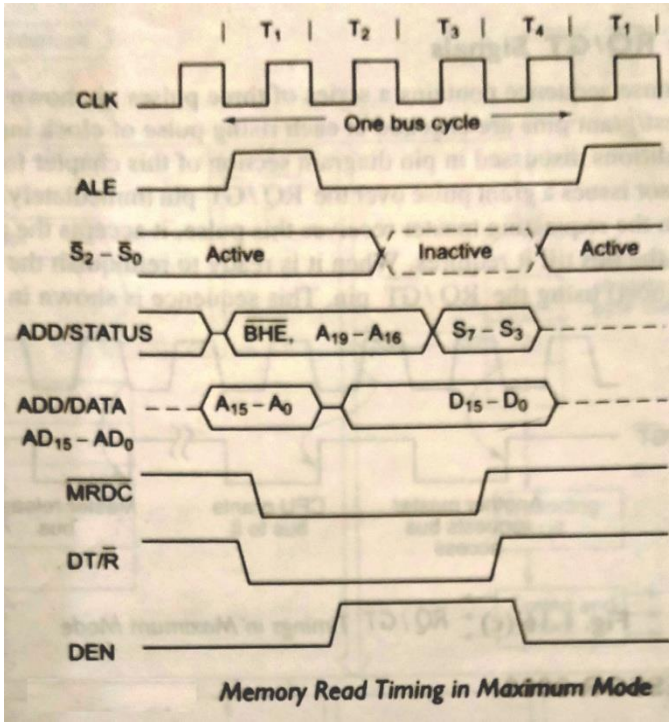
Long type questions [7 marks each]

Q-1) **Explain concept of maximum mode 8086 system and timings. [S-16(Q1-c)], [S-17(Q2-b)]**

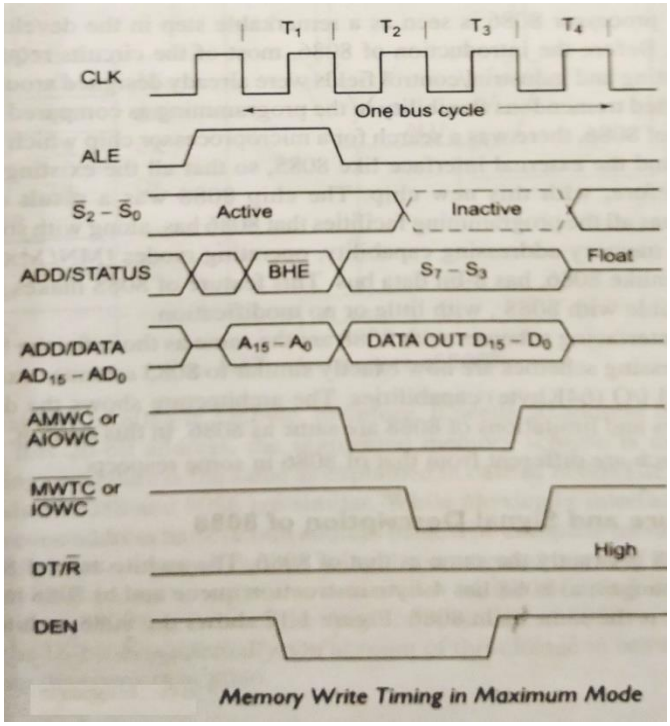
Ans:- In the maximum mode, the 8086 is operated by strapping MN/MX pin to ground. In this mode, the processor derives the status signals $\overline{S_2}$, S_1 and S_0. Another chip called bus controller derives the control signals using this status information.

The basic function of IC 8288, is to derive control signals like $\overline{RD}$ & $\overline{WR}$, $\overline{DEN}$, DT/$\overline{R}$, ALE, etc. It has i/p lines $\overline{S_2}$, $\overline{S_1}$& $\overline{S_0}$and CLK, which are driven by the CPU. It derives the o/p$_s$ ALE, DEN, DT/$\overline{R}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{AIOWC}$.

The maximum mode system timing diagrams are also divided in two portions as read(i/p) and write(o/p).



Memory Read Timing in Maximum Mode

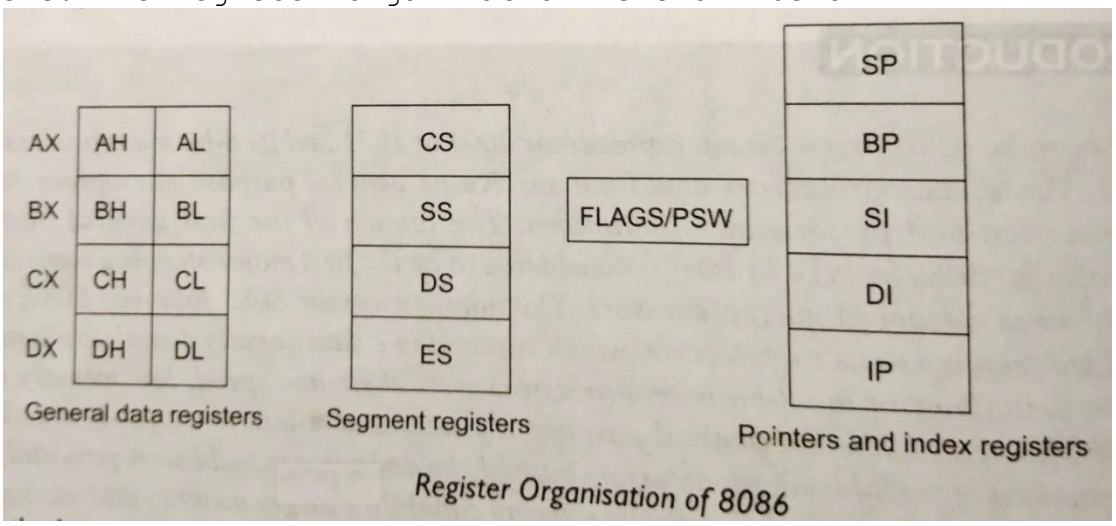


Memory Write Timing in Maximum Mode

The address/data and address/status timings are similar to the minimum mode. ALE is asserted in T_1,just like minimum mode. The only difference lies in the status signals used and available control and advanced command signals. The above figure shows the timings of read and write operation. The CS logic block represents chip select logic and 'e' or 'O' suffixes indicate even and odd address memory bank.

Q-2) **Describe the register organization of 8086. [S-17(Q2-c)]**

Ans:- The register organization of 8086 μP consists of general data registers, segment registers, flag register and pointers & index registers. The register organization is shown below –



Register Organisation of 8086

The register AX, BX, CX and DX are the general purpose 16-bit registers. The GPR, can be used as either 8-bit or 16-bit registers. They may be either used for holding data, variables and inermediate results temporarily or for other purposes like a counter or for storing offset address for some particular addressing modes etc. AX is used as 16-bit accumulator. The lower 8-bit as AL can be used as 8-bit accumulator for 8-bit operation. The register CX is used as a default counter in case of string and loop instructions. BX is used as an offset storage for forming physical addresses. DX is used as an implicit operand or destination of instructions.

There are 4 segment registers- Code segment(CS), Data segment(DS), Extra segment(ES) and Stack sement(SS). The CS register is used for addressing a memory location in the code segment of memory where program is stored. The DS register points to the data segment of memory where data is resided. The ES also contains the data. The SS register is used for addressing stack segment of memory, which store the stack.

The pointers contain offset within the particular segments. The pointers IP, BP and SP usually contain offsets within the code(IP) and stack(BP & SP). The index regesters are used as GPR as well as for offset storage in case of indexed, based indexed or relative based indexed addressing modes. The register SI is used to store the offset of source data in data segment while DI is used to store the offset or destination in DS or ES. The index registers are paricularly useful for string manipulation.

The 8086 μP flag register contents indicate the results of computations in the ALU. It also contains some flag bit to control the CPU operations. It is devided in two parts- condition cor or status flags and machine control flags.

Chapter-II

(80286/80287- A Microprocessor with Memory Management & Protection)

Short type questions [2 marks each]

Q-1) **What is the function of cap pin in 80286? [S-16(Q2-a)]**
Ans:- A 0.047µF, 12V capacitor is connected between this i/p pin and ground to filter the o/p of the internal substrate bias generator.

Q-2) **Define PVAM. [S-16(Q3-a)]**
Ans:- Protected Virtual Address Mode(PVAM) is the addressing mode used by 80286 µP which supports the concepts of virtual memory and memory management. The concept of virtually memory is implemented using physical memory that the CPU can directly access and secondary memory that is used as a storage for data and program.

Q-3) **What is function of Coprocessor? [S-17(Q3-a)]**
Ans:- The coprocessor is designed to operate with the other processor by adding med instructions to offer numeric processing capabilities the other processors. They support integer, floating point, BCD, trigonometric and logarithm calculations.

Q-4) **Define Privilege. [S-17(Q4-a)], [W-17(Q2-a)]**
Ans:- The privilege is a four level hierarchical mechanism to control the access to descriptors. It provides protection within a task. It offer or denies access to a segment at the behest of the descriptors.

Medium type questions [5 marks each]

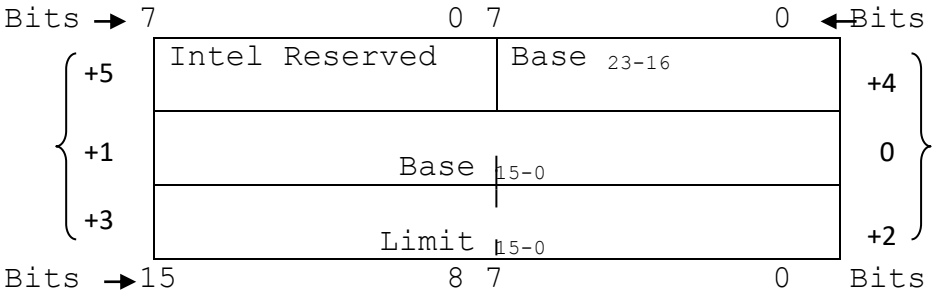
Q-1) **Explain briefly about protection and privilege.[S-16(Q2-b)]**
Ans:- **Protection:-**The 80286 can utilize its privilege mechanism for protecting its data or code from unwanted accesses. The 80286 supports the 3 basic mechanisms to provide protection –

a. ***Restricted use of segments:-*** This is accomplished with the help of read/write privilege. The segment uses are restricted by classifying the corresponding descriptions under LDT & GDT.

b. ***Restricted accessesto segments:-*** This is accomplished using descriptor usages limitations and the rules of privilege check, DPL, TPL & CPL.

c. ***Privileged Instructions:-*** These are to be executed or carried out at certain privilege levels determined by CPL & I/O privilege level(IOPL).

Privilege:- The 80286 supports a four level hierarchical privilege mechanism to control the access to descriptors and hence to the corresponding segments of the task. The control of the access to descriptors results in the prevention of unwanted or undue access to any of the code or data segments or unintentional interference in the higher privilege level tasks. The privilege mechanism offers or denies access to a segment at the behest of the privilege bits of the corresponding descriptor.



Q-2) **Explain Protected Virtual Addressing Mode (PVAM) with physical address calculation. [S-17(Q3-b)]**

Ans:-

In PVAM, the 80286 uses the 16-bit content of a segment register as a selector to address a descriptor stored in physical memory. The descriptor is a block of contiguous memory locations containing information of base address, limit, type of segment, privilege level etc. The base address (i.e) the starting location of a segment and segment limit indicates the maximum size of segment. Thus using these two, the last location of the segment is determined. The privilege level offers protection to the segment from unauthorized accesses. A descriptor stores the information of a certain segment may or may not be present in physical memory at a given time instant. Also, the information whether the segment has been accessed by another task in the past, is also stored in segment descriptor. This information helps in deciding the segment should be unswapped from the physical memory or not. The segment base address is a 24-bit pointer that addresses the first location in that segment which is added with 16-bit offset to calculate a 24-bit physical address. The maximum segment size will be of 64 Kbyte since the offset is only of 16-bits.

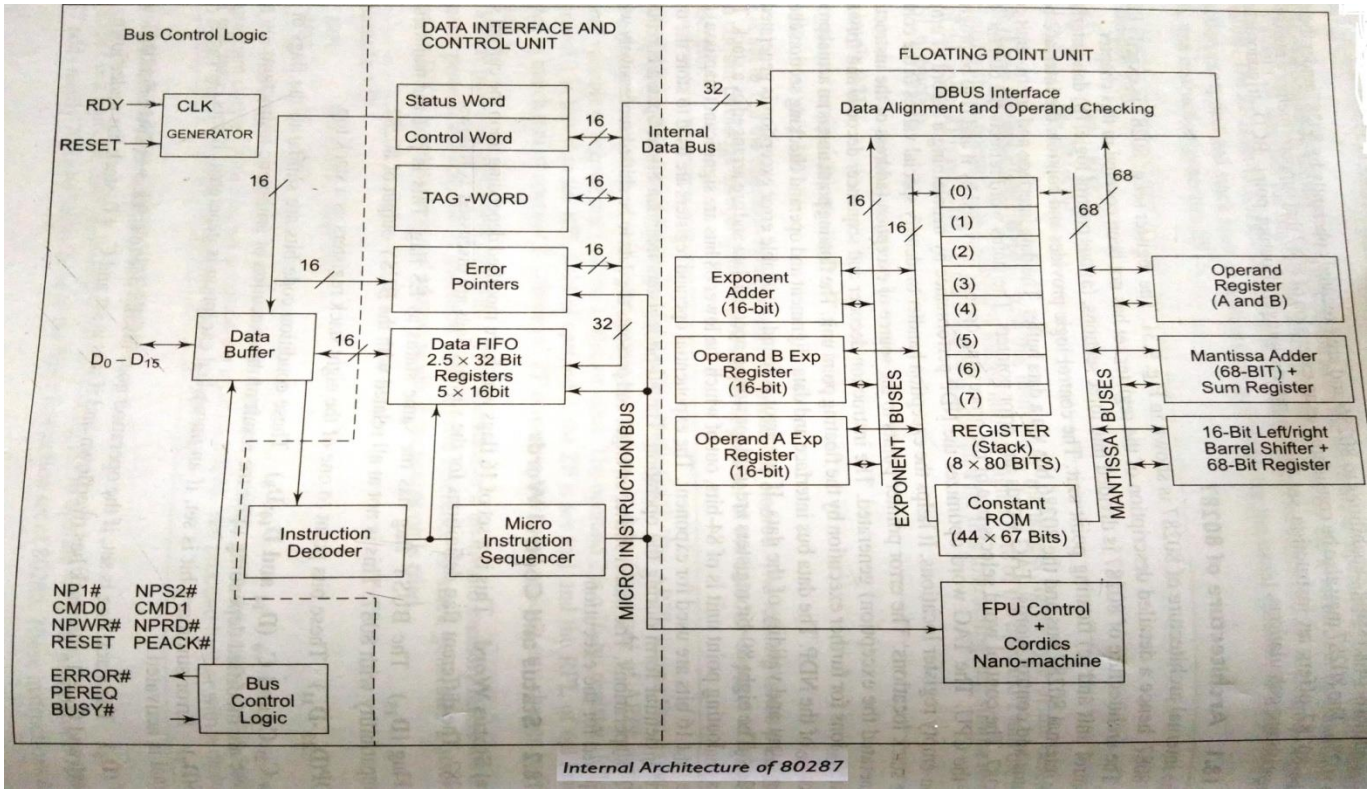
Q-3)**Write a short note on 80287 math coprocessor. [W-17(Q2-b)]**

Ans:- The 80287 is a numeric data processor specially designed to operate with the processor 80286. The 80287 adds nearly 70 more instructions to the basic instruction set of 80286. These instructions mainly offer numeric processing capabilities to 80286 and are executed coherently by 80287 under the control of 80286. The 80287 may also be considered as an extension of 8087 that supports memory management. The 80287 offers an instruction set that supports integer, floating point, BCD, trigonometric and logarithmic calculations.

It interface with 80286 system using a set of 10 pins, namely PEREQ, PEACK#, BUSY#, ERROR#, NPRD#, NPWR#, NPS1#, NPS0#, CMD0 and CMD1. The 80287 supports seven data types.

Q-4) **Draw the internal block diagram of 80287 Math coprocessor and explain important task. [S-16(Q3-b)], [S-17(Q4-b)]**

Ans:- The internal architecture of 80287 Math coprocessor is given below-



Internal Architecture of 80287

The architecture is divided into 3 sections- Bus control logic, Data interface and control unit, Floating point unit.

The control logic provides and controls the interface between the internal 80287 bus and the 80286 bus via a data buffer. The data interface and control unit contains status and control words, TAG words and error pointers. The status word reflects the current status of 80287. The control word selects one of the processing options provided by it and is to be programmed by the CPU. The TAG word optimizes the NDP performance by maintain a record of empty and non empty register locations. The instruction decoder and sequencer decodes and forwards he instructions for further execution by the floating point unit. The FPU is an actual processing section of NDP. The data bus interface and data alignment and operand checking section checks the alignment and validity of the data. The exponential operand registers are used to store the operands in exponential form during the operation. The barrel shifter arranges and presents the data to be shifted successively whenever required for the execution.

Q-5)**Write down the function of following signals in 80286. [S-19(Q2-b)]**

(i) PEREQ

(ii) PEACK

(iii) BUSY

(iv) $\overline{\text{ERROR}}$

(v) CAP

Ans:-

The functions of the following signals in 80286-

PEREQ:- The PEREQ input requests the 80286 to perform a data transfer for a processor extension.

$\overline{\text{PEACK}}$:- This active low output indicates to the processor extension that the requested operand is being transferred.

$\overline{\text{BUSY}}$:- This input goes low, indicating the 80286 to suspend the execution and wait until this signal becomes inactive. When it is high, indicates the 80286 to continue with the program execution.

$\overline{\text{ERROR}}$:- An active $\overline{\text{ERROR}}$ signal causes the 80286 to perform the processor extension interrupt while executing the WAIT and ESC instruction. This indicates to 80286 that the processor extension has committed a mistake and hence it is reactivating the processor extension interrupt.

CAP:- A 0.047μf, 12V capacitor is connected between this input pin and ground to filter the output of the internal substrate bias generator.

Q-6) **Discuss about descriptors and their types of 80286. [S-19(Q3-b)]**

Ans:- In general, descriptors carry all the relevant information regarding a segment and its access rights. The 80286 has segment descriptors for code, stack and data segments as basic descriptors. It has system control descriptors for special system data segments and control transfer operations. Each descriptor is 8-btes long.

A code or data segment descriptor contains 16-bit segment limit, 24-bit segment base address, 8-bit access rights byte and the remaining 16-bits are reserved for upward compatibility. Code segment descriptors are used to refer code segments and data segment descriptors are used to refer data segments. If the S bit in the access bytes is '1', the descriptor is either code or data segment descriptor. If the E bit is 1 then it indicates code segment and if E=0, it indicates data segment.

If the S=0, the system segment descriptor is selected. It is used to store system data and execution state of a task. The system segment descriptors are of 7 types. The types 1 to 3 are called system descriptors and the types 4 to 7 are called gate descriptor as they are used to control the access of entry points within the code to be executed. There are 4-types of gate descriptor- call gate, task gate, interrupt gate and trap gate.

Q-7) **What is the use of privilege types? Explain the following terms. [S-19(Q6-b)]**

(i) Task Privilege
(ii) Descriptor Privilege
(iii) Selector Privilege

Ans:- The privilege types is used to control the access to descriptors and hence to the corresponding segments of the task.

(i) **Task Privilege:-** Each task is assigned a privilege level, which indicates the priority of the task. The task privilege at that instant is called the current privilege level(CPL). CPL is defined by the lower order two bits of the CS register for an executable segment. The task begins execution at the selected CPL values specified by the CS.

(ii) **Descriptor Privilege:-** The descriptor privilege is specified by the DPL field of the access rights byte. The DPL specifies the least task privilege level(CPL) that may be used to refer to the descriptor. Hence, the task with privilege level 0, can refer to all the lower level privilege descriptors. However, the task with privilege level 3 can refer to only level 3 descriptors. This rule applies to all the descriptors except the LDT descriptors.

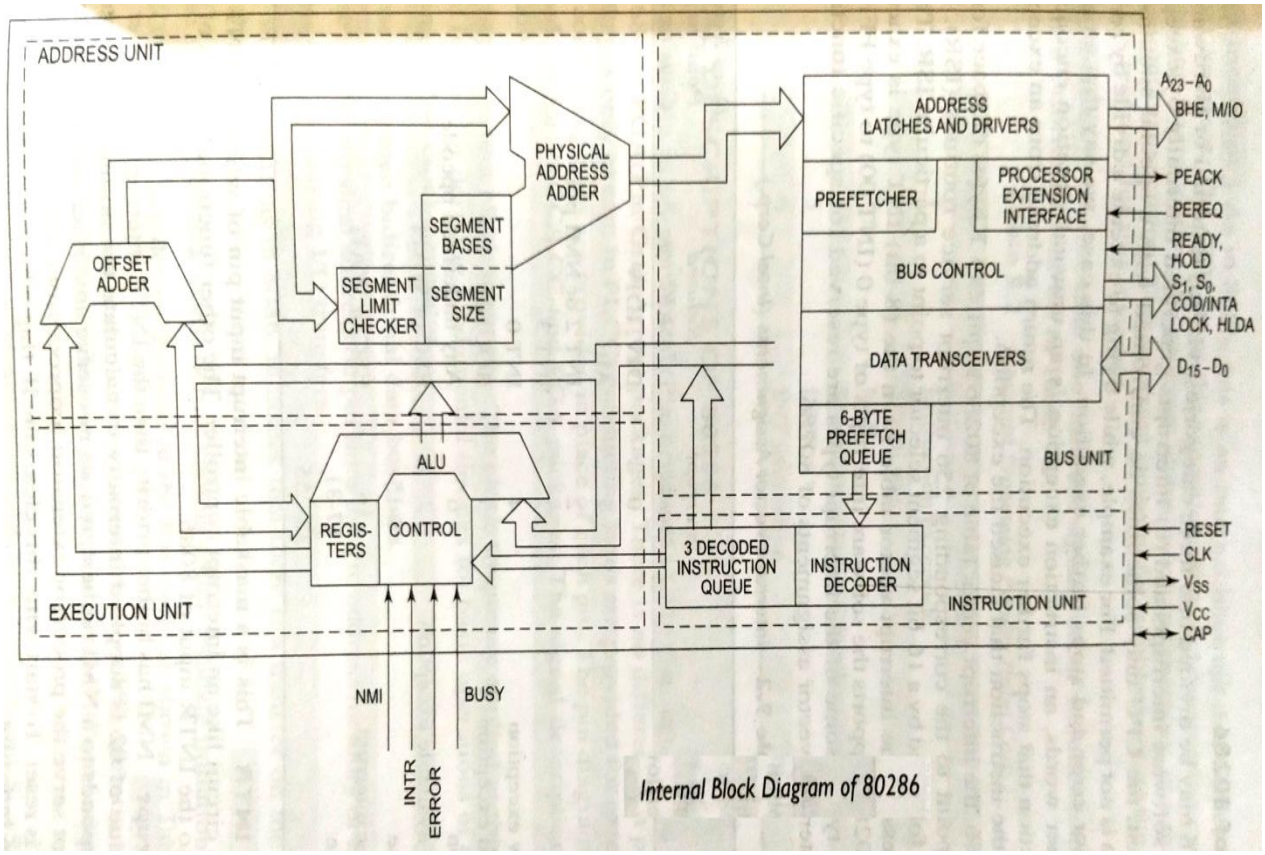
(iii) **Selector Privilege:-** This privilege is specified by the RPL field of a segment register. A selector RPL may use a less trusted privilege than

the current privilege level for the further use. This is known as the effective privilege level(EPL) of the task. The EPL is thus the maximum of RPL and CPL. The RPL is used to ensure that the pointer parameters passed to a more privileged procedure are not given the access of data at the privilege higher than the caller routine. The pointer testing instructions are used for this purpose.

Long type questions [7 marks each]

Q-1) **Draw the internal architecture of 80286 by a neat block diagram and explain its function. [S-16(Q2-c)], [S-17(Q2-c)], [W-17(Q2-c)]**

Ans:-

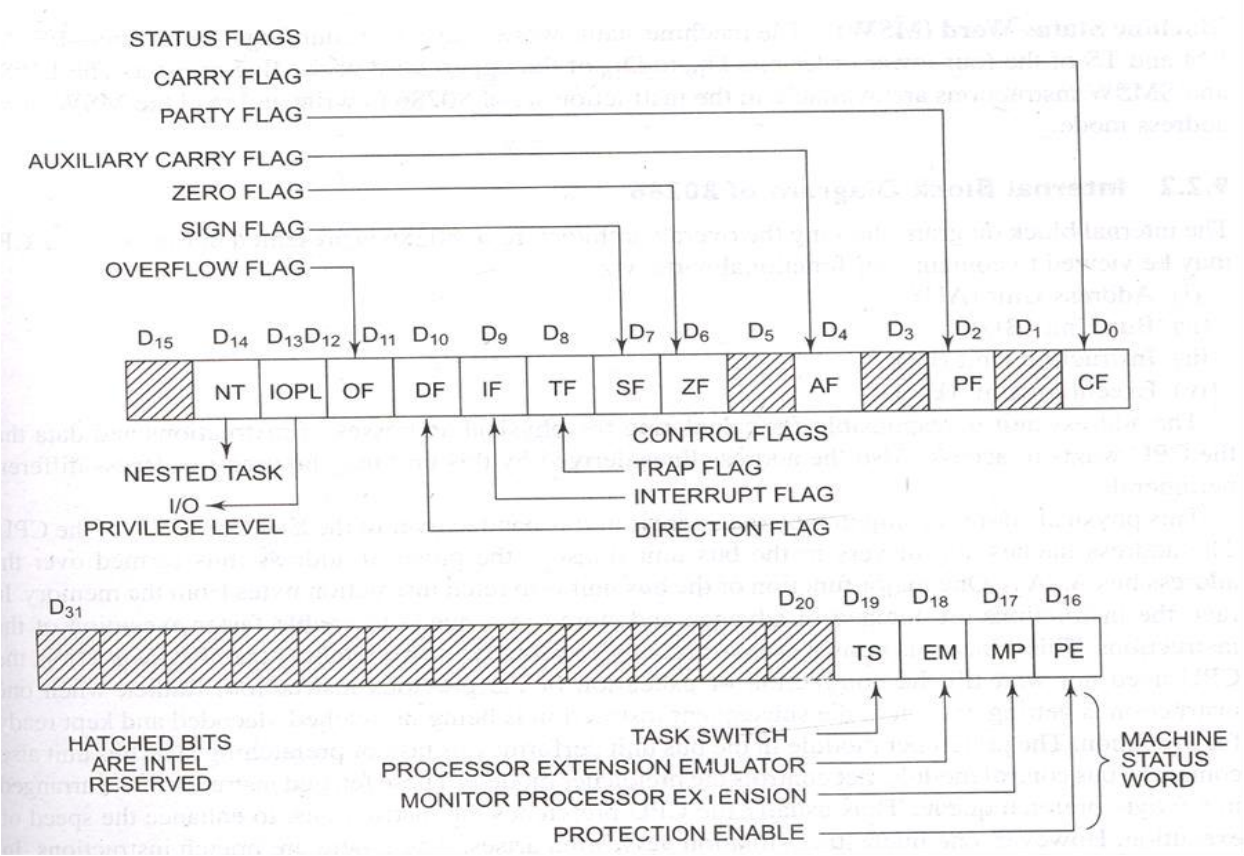


The internal block diagram is viewed to contain 4 parts-

a. ***Address Unit(AU):-*** The address unit is responsible for calculating the physical addresses of instructions and data that the CPU wants to access. Also the address lines derived by this unit may be used to address different peripherals.
b. ***Bus Unit(BU):-*** The physical address computed by AU is handed over to BU. The address latches and drivers in the BU transmit the physical address formed address bus Ao-A23. BU fetches instruction bytes from memory. The BU also contains a bus control module which controls the prefetcher module.
c. ***Instruction Unit(IU):-*** The 6-byte prefetch queue forwards the instructions arranged in it to IU. The IU accepts instructions from the prefetch queue and instruction decoder decodes them one by one.
d. ***Execution Unit(IU):-*** The o/p of the decoding ckt. drives a control ckt. in the EU, which is responsible for executing the instructions received from the decoded instruction queue, which sends the data part of the instruction over the data bus. The register bank of EU is used for storing the data and ALU, carries out all the operations.

Q-2) **Draw the diagram and explain the flag register of 80286. [S-19(Q2-c)]**

Ans:- The flag register of 80286 is shown in the figure below. The flag register reflects the results of logical and arithmetic instructions. The flag register bits D_0, D_2, D_4, D_6, D_7 and D_{11} are modified according to the result of the execution of logical and arithmetic instructions. These are called as status flag bits. The bits D8 and D9 namely, TF and IF bits, are used for controlling machine operation and thus they are called control flags.



The additional field available in 80286 flag register are, IOPL-I/O privilege field (D_{12} and D_{13}), NT-Nested task flag(D_{14}), PE-protection enable(D_{16}), MP-monitor processor extension(D_{17}), processor extension emulator(D_{18}) and TS-task switch(D_{19}). The four flags-PE,MP,EM and TS forms the machine status word(MSW).

Chapter-III

(80386/80387 And 80486- The 32-bit Processor)

Short type questions [2 marks each]

Q-1)**Write any two salient features of 80386DX. [S-16(Q4-a)]**
Ans:- The two salient features of 80386DX are-

(i) With its 32-bit address bus, the 80386 can address up to 4Gbystes of physical memory.

(ii) It supports 16k (16384)number of segments and thus the total virtual memory space is 4GB X 16k= 64 terabytes. Also, it supports 8-bit/16-bit/32-bit data operands.

Q-2) **Define Packed BCD. [S-17(Q5-a)]**
Ans:- Packed BCD represents two packed BCD digits using a byte (i.e) from 00 to 99.

Q-3) **What is Virtual mode? [S-17(Q6-a)]**
Ans:- Virtual mode is an virtual 8086 operating environment to execute the 8086 programs in protected mode of 80386. In virtual mode 8086 can address 1Mbytes of physical memory that may be anywhere in the 4Gbytes address space of the protected mode of 80386. The paging mechanism and protection capabilities are available in this mode.

Q-4) **Write down the data types of 80386. [W-17(Q3-a)], [S-19(Q4-a)]**
Ans:- The 80386 supports 17 data types. They are-

1) Bit
2) Bit Field
3) Bit String
4) Signed Byte
5) Unsigned Byte
6) Integer word
7) Long Integer
8) Unsigned Integer word
9) Unsigned Long Integer
10) Signed Quad word
11) Unsigned Quad word
12) Offset
13) Pointer
14) Character
15) Strings
16) BCD
17) Packed BCD

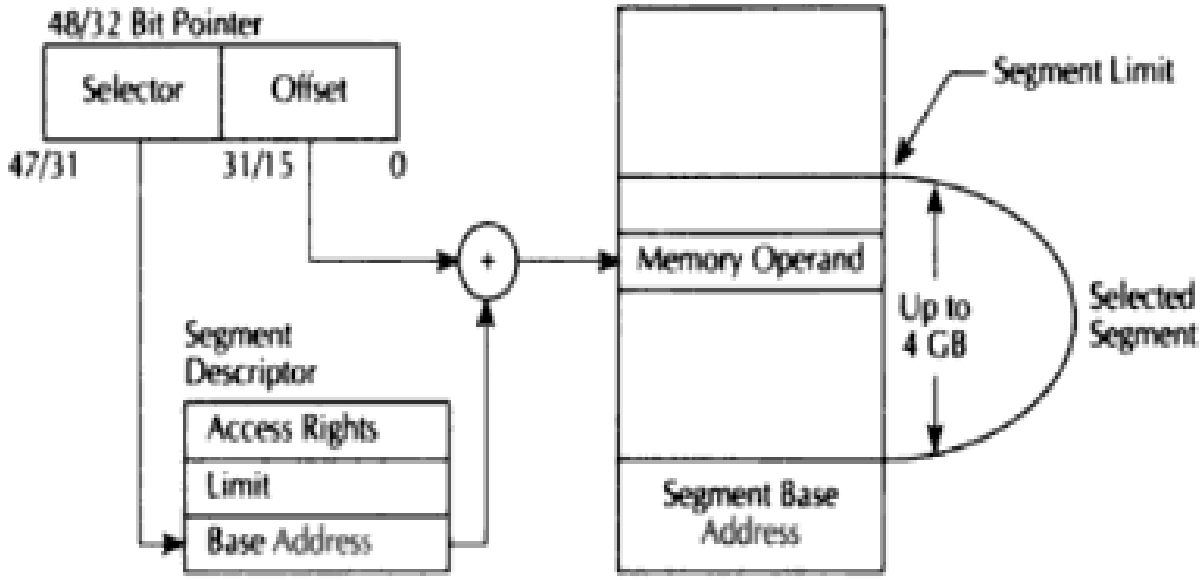
Medium type questions [5 marks each]

Q-1) **Explain briefly about paging operation. [S-16(Q2-b)]**

Ans:- Paging is one of the memory management techniques used for virtual memory multitasking operating systems. Paging divides the memory into fixed size pages. Pages do not have any logical relation with the program. The pages are just the fixed size portions of the program module or data. The advantage of the paging is that the complete segment of a task need not be in the physical memory at any time. Only a few pages of the segments, which are required currently for the execution need to be available in the physical memory. Whenever the other pages of the task are required for execution, they may be fetched from the secondary storage. The previous pages which are executed, need not be Available in the memory and hence the space occupied by them may be relinquished for other tasks.

Q-2) **Explain protected mode of 80386. [S-17(Q5-b)]**

Ans:- In protected mode, the 80386 can address 4Gbytes of physical memory and 64-TBytes of virtual memory per task. In this mode, the contents of segment registers are used as selectors to address descriptors which contain the segment limit, base address and access rights byte of the segment. The offset is added with segment base address to calculate linear address. This linear address is further used as physical address, if the paging unit is disabled, else it will be convert the linear address into physical.



Paging unit is a memory management unit enabled only in this mode. The paging mechanism allows handling of large segments of memory in terms of pages of 4Kb size. The paging unit operates under the control of segmentation unit. The protected mode allows the use of additional instructions, addressing modes and capabilities of 80386.

Q-3) **Explain addressing modes of 80386. [W-17(Q5-b)]**

Ans:- The 80386 supports eleven addressing modes to facilitate efficient execution of higher level language programs. The 80386 has all addressing modes that are available with 80286. In these modes, 80386 can now have 32-bit immediate or 32-bit register operands or displacements. Beside these, 80386 has a family of scaled modes. In case of the scaled modes, any of the index register values can be multiplied

by a valid scale factor to obtain the displacement. The valid scale factors are 1,2,4 and 8.

The different scaled modes are –

SCALED INDEDXED MODE:- Contents of an index register are multiplied by a scale factor that may be added further to get the operand offset.

```
MOV EBX, LIST [ESI*2] List displacement
MUL ECX, LIST [EBP*4]
```

BASED SCALED INDEDXED MODE:- Contents of an index register are multiplied by a scale factor and then added to base register to obtain the offset.

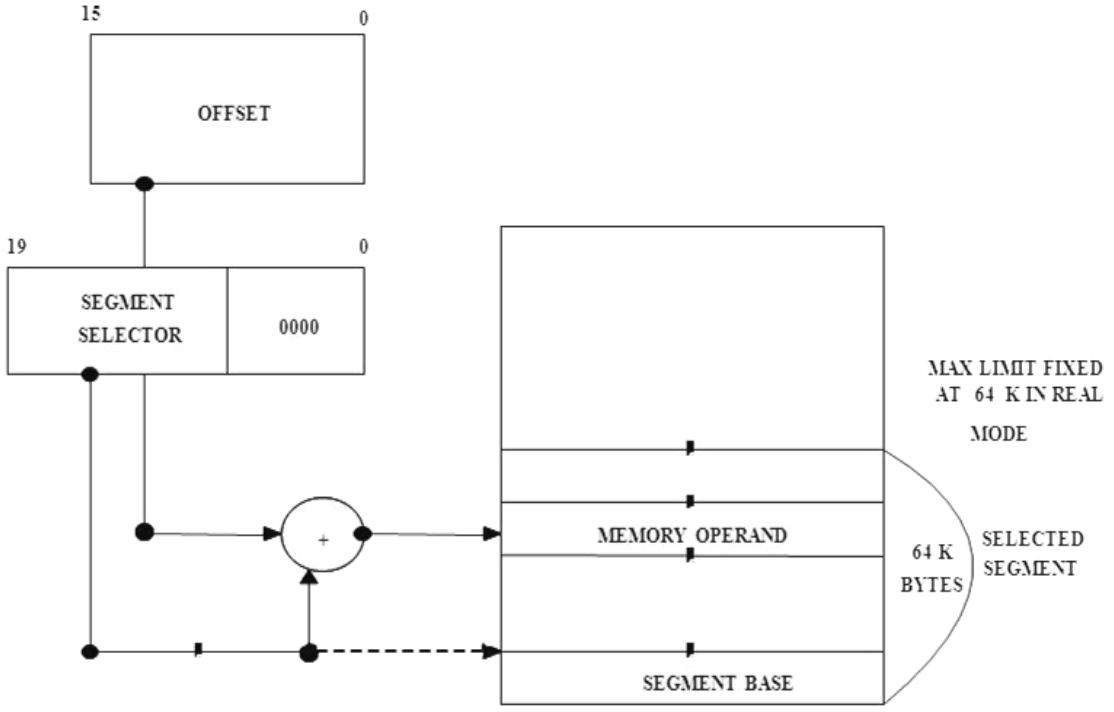
```
MOV EBX, [EDX*4][ECX]
MOV EAX, [EBX*2][ECX]
```

BASED SCALED INDEDXED MODE with DISPLACEMENT:- Contents of an index register are multiplied by a scaling factor and the result is added to a base register and a displacement to get the offset of an operand.

```
MOV EAX, LIST [ESI*2][EBX + 0800]
MUL EBX, LIST [EDI*8][ECX + 0100]
```

Q-4) **Explain real address mode of 80386. [S-19(Q4-b)]**

Ans:-



After reset, the 80386 starts from the memory location FFFFFFF0 H under the real address mode. In this mode, it works as a fast 8086 with 32-bit registers and data types. The addressing techniques, memory size, interrupt handling in this mode are similar to that of 80286. All the instructions of 80386 are available in this mode except those are designed to work with or for protected mode. In this mode, the default operand size is 16-bit but 32-bit operands and addressing modes may be used. The segment size in real mode is 64K. Hence, the real mode initializes the 80386 and prepares it for protected mode.

In this mode, the 80386 can address at the most 1MB of physical memory using addressing lines A_0-A_9. Paging unit is disabled in this mode, hence, the real addresses are same as the physical addresses.

Q-5) **Name the types of data types of 80486 and discuss each data type. [S-19(Q7-b)]**
Ans:- The 80486 CPU supports 7 types of data type including floating point data types. FPU does not support any unsigned data type.

i)Signed/unsigned Data Type:- 8-bit, 16-bit, 32-bit signed and unsigned integers are supported by 80486 while the FPU supports 16-bit, 32-bit, 64-bit signed data.

ii)Floating Point Data Types:- Single precision, double precision, extended precision real data are supported by the FPU.

iii)BCD Data Types:- Packed and unpacked BCD data types. The CPU supports 8-bit packed and unpacked data types. The FPU supports 80-bit packed BCD data types.

iv)String Data Types:- Strings of bits, bytes, words and double words are supported by the CPU. Each of the strings may contain up to 4Gbytes.

v)ASCII Data Type:- The ASCII representation of the characters are supported by 80486.

vi)Pointer Data Types:- 48-bit pointers containing 32-bit offset at the least significant bits and 16-bit selector at the most significant bits are supported by the CPU. Also 32-bit pointers containing 32-bit offsets are supported by the CPU.

vii)Little Endian and Big Endian Data Types:- The 80486 uses the Little Endian data format which means for a data of size bigger than one byte, the least significant byte is stored at the lowest memory address while the most significant byte is stored at the highest memory address. The complete data is referred to by the lowest memory address.

The Big Endian data format allows the storage of data in the exactly opposite manner(i.e)the MSB is stored in the lowest memory address, while the LSB is stored in highest memory address.

Long type questions [7 marks each]

Q-1) **Explain the Register Organisation of 80386. [S-16(Q3-c)], [W-17(Q3-b)]**
Ans:- The 80386 has eight 32-bit registers which may even be used either as 8-bit or 16-bit registers. A 32-bit register known as an extended register, represented by the register name with a prefix E. As EAX, EBX,EBP, ESI, ESP, EDI etc.

There are six segment registers available in 80386 as CS, SS, DS, ES, FS and GS. The CS and SS are the code and stack segment register while DS, ES, FS and GS are the four data segment registers.

Flag Register:- The flag register of 80386 is a 32-bit register. Out of which bits D_{18} to D_{31}, D_{15}, D_5 and D_3 are reserved while D_1 is always set at 1. The lower 15 bits (D_0-D_{14}) are same as of 80286. Only two extra new flags are added VM and RF which are derive the flag register of 80386.
If the VM is set, 80386 enters the virtual 8086 mode within the protected mode. This bit is set using the IRET instruction. RF flag is used with the debug register breakpoints. It is checked at the starting of every instruction cycle and if it is set, any debug fault is ignored

during the instruction cycle. The RF is automatically reset after successful execution of every instruction, except for the IRET and POPF instruction.

Segment Descriptor Register:- The segment descriptor registers of 80386 are not available for programmers, rather, they are internally used to store the descriptor information, like attributes, limit and base addresses of segments. The six segment registers have corresponding six 73-bit descriptors register. Each of them contains 32-bit base address, 32-bit base limit and 9-bit attributes. The segment registers are CS, SS, DS, ES, FS and GS.

Control Register:- The 80386 has three 32-bit control registers CR_0, CR_2 and CR_3 to hold global machine status independent of the executed task. The load and store instructions are available to access these registers. The control register CR_1 is reserved for use in future processors.

System Address Register:- Four special registers are defined to refer to the descriptor tales supported by 80386(i.e) Global Descriptor Table(GDT), Interrupt Descriptor Table(IDT), Local Descriptor Table(LDT) and Task State Segment Descriptor(TSS). The system address register and system segment registers hold the addresses of these descriptor tables and the corresponding segments. These registers are known as GDTR, IDTR, LDTR and TR respectively. The GDTR and IDTR are called as system address and LDTR & TR are called as system segment registers.

Debug & Test Register:- The 80386 provide a set of eight debug registers for hardware debugging. Out of these(DR_0-DR_7), two registers DR_4 and DR_5 are reserved. The initial four registers DR_0-DR_3 store four program controllable breakpoint addresses; while DR_6 & DR_7 hold breakpoint status and breakpoint control information. Test control and Test status registers provide page cacheing.

Q-2) **Explain briefly Enhanced instruction set of 80386. [S-16(Q4-c)], [S-19(Q4-c)]**

Ans:- The instruction set of 80386 contains all the instructions supported by 80286. The enhanced instruction set of 80386 are categorized as-

Bit Scan Instructions:- 80386 instruction set has two bit scan mnemonics(i.e) BSF(Bit Scan Forward) and BSR(Bit Scan Reverse). Both of these instructions scan the operand for a '1'bit, without actually rotating it. The BSF instruction scans the operand from right to left. If a'1' is encountered, zero flag is set and the bit position of '1' is stored into the destination operand. If no, then zero flag is reset. The BSR instruction perform the same but scans the operand from left to right.

Bit Test Instructions:- 80386 has four bit test instructions(i.e) BT(Test a bit), BTC(Test a bit & complement), BTR(Test & reset a bit), and BTS(Test and set a bit). All these instruction test a bit position in the destination operand, specified by the source operand.

If the bit position of the destination operand specified by the source operand satisfies the condition specified in the mnemonic, the carry flag is affected appropriately.

Conditional Set Byte Instructions:- This instruction sets all the operand bits, if the condition specified by the mnemonic is true. This instruction group has 16 mnemonics corresponding to 16 conditions. These are- SETO, SETNO, SETB/SETNAE, SETNB/SETAAE, SETE/SETZ, SETNE/SETNZ, SETBE/SETNA, SETNBE/SETA, SETS, SETNS, SETP/SETPE, SETNP, SETL/SETNGE, SETNL/SETGE, SETLE/SETNG, SETNLE/SETG.

Shift Double Instructions:- These instructions shift the specified number of bits from the source operand into the destination operand. The 80386 instruction set has two mnemonics(i.e)SHLD(Shift double left) and SHRD(Shift right double). The SHLD shifts the specified number of bits from the upper side(i.e)MSB of the source operand into the lower side or LSB of the operand. The SHRD do the same but from LSB of source operand to MSB of destination operand.

Control Transfer Instructions:- The 80386 has a set of instruction for intersegment jumps and are executed only in protected mode. These are used to transfer the control either at the same privilege or at a different privilege level. The corresponding RET instructions are also available to switch back from the new task initiated by CALL, JMP or INT instructions to the parent task.

Q-3) **Explain addressing modes of 80387 with examples. [S-17(Q4-c)]**
Ans:- It is CPU on a single chip

Q-4) **Define paging and its operation with tables, directory and mechanism. [S-17(Q5-c)]**
Ans:- It is CPU on a single chip

Q-5)**Discuss about segmentation and paging. [W-17(Q3-c)]**
Ans:-It is CPU on a single chip

Chapter-IV

(Recent Advance in Microprocessor Architecture- A Journey from Pentium Onwards)

Short type questions [2 marks each]

Q-1) **Define Branch Prediction. [S-16(Q5-a)]**

Ans:-It is CPU on a single chip. It includes the ALUL, small memory, register arrays on a single chip. It is of 8-bit, 16-bit or 32-bit type processor.

Q-2) **What is MMX instruction sets? [S-17(Q7-a)]**

Ans:- MMX(multimedia extension) instruction set has 57 MMX instructions. These are used to write efficient programs for image filtering, enhancement, coding and other algorithms. Example- PADD(B,W,D); PSUB; PCMPEQ, etc.

Q-4) **What is MMX? [W-17(Q4-a)]**

Ans:- MMX(multimedia extension) is a technology which is used to write efficient programs for image filtering, enhancement, coding and other algorithms.

Medium type questions [5 marks each]

Q-1) **What is MMX and explain the intel MMX architecture with a neat block diagram. [S-16(Q5-b)], [W-17(Q5-c)]**

Ans:-**Microprocessor:-** It is CPU on a single chip.

Chapter-V

(PENTIUM 4- Processor of the New Millenium)

Short type questions [2 marks each]

Q-1)**What is Hyper threading Technology? [S-16(Q6-a)], [W-17(Q5-a)]**

Ans:-It is CPU on a single chip. It includes the ALUL, small memory, register arrays on a single chip. It is of 8-bit, 16-bit or 32-bit type processor.

Q-2)**Write down two important feature of Pentium 4. [W-17(Q6-a)], [S-19(Q5-a)]**

Ans:- The two important feature of P-IV are-

- It is based on NetBurst microarchitecture.
- It has 42 million transistors, fabricated using 0.18 micron CMOS process.

Medium type questions [5 marks each]

Q-1) **What is hyperthreading technology? Explain briefly. [S-16(Q6-b)], [S-19(Q5-c)]**

Ans:- Hyperthreading technology is a groundbreaking technology to improve processor performance. It allows software programs to 'see' two processors and work more efficiently.

This new technology enables the processor to execute two series, or threads of instructions at the same time, thereby improving performance and system responsiveness. HT technology requires a computer system with an Intel Pentium-4 processor supporting HT technology and a HT technology enabled chipset, BIOS and operating system.

Each process has a context in which all the information related with the current state of execution of the process are described. Each process contains at least one threads and sometime more than one thread is present in a process. Each thread has its own local context. Also the process has a context which is shared by all the threads in that process. The features of HT technology are given below-

- HT makes a single physical processor appear as multiple logical processors.
- Each logical processor has its own architecture state where a set of single execution units are shared between logical processors.
- HT allows a single processor to fetch and execute two separate code streams simultaneously.
- In most of the applications, the physical unit is shared by two logical units.

Q-2) **Explain salient features of Pentium 4. [S-17(Q6-b)]**

Ans:- Some of the features of Pentium-4 are-

- It is based on NetBurst microarchitecture.
- It has 42 million transistors, fabricated using 0.18 micron CMOS process.
- Its die size is 217 sq. mm. and power consumption is 50W.
- Clock speed varies from 1.4GHz to 1.7GHz. At 1.5GHz the microprocessor delivers 535 SPECint2000 and 558 SPECfp2000 of performance.

- It has hyper-pipelined technology- Its pipeline depth extends to 20 stages.
- In addition to the L1, 8KB data cache, it also includes an execution trace cache(ETC) that stores up to 12K decoded micro-ops in the order to program execution.
- The on-die 256KB L2-cache is non blocking, 8-way set associative. It employs 256-bit interface that delivers data transfer rates of 48 GB/s at 1.5GHz.
- Pentium-4 NetBurst microarchitecture introduces Internet Streaming SIMD Extensions2 (SSF2) instructions. This extends the SIMD capabilities that MMX technology and SSF technology delivered by adding 144 new instructions.
- It supports 400MHz system bus, which provides up to 3.2GB/s of bandwidth. The bus is fed by dual PC800 Rambus channel.
- Two arithmetic logic units(ALUs) on the Pentium4 processor are clocked at twice the core processor frequency.
- Advanced dynamic execution.

Q-3) **Write down the enhanced instruction set of Pentium. [W-17(Q4-b)]**
Ans:-It is CPU on a single chip. It

Q-4) **With proper diagram explain memory subsystem. [W-17(Q6-b)]**
Ans:-It is CPU on a single chip

Q-5) **Discuss the front end module of Pentium 4 processor. [S-19(Q5-b)]**
Ans:- The Front end module of Pentium-4 processor contains- (i)IA 32 Instruction decoder (ii)Trace Cache (iii)Microcode ROM and (iv)Front End branch predictor. The basic function of the front end module is to fetch the instructions to be executed, decode them and feed decoded instructions to the next module, which is the out of order execution module.

IA 32 Instruction Decoder:- The role of instruction decoder is to decode the instructions of variable length and supported by many addressing modes concurrently and translate them into micro-operations known as μops. A single instruction decoder decodes one instruction per clock cycle. Some are translated into single μop while others are into multiple μops.

In case of a complex instruction, when the instruction needs to be translated into more than four μops, the decoder usually does not decode such instructions. It transfers the task to a Microcode ROM.

Trace Cache (TC):- The special instruction cache is known as Trace Cache, which is a special feature of Pentium-4 micro architecture. It is special because it does not store the instructions but the decoded stream of instructions. The Trace cache can store up to 12K μops. The cache assembles the decoded μops into ordered sequence of μops called Traces. A single trace has many Trace lines and each Trace line has six μops.

Microcode ROM:- When some complex instructions like interrupt handling or string manipulation appear, the Trace cache transfer the control to a Microcode ROM, which stores the μops corresponding to these complex instructions. When the control is passed to the Microcode ROM, the corresponding μops are issued. After the μops delivered by the trace cache and the Microcode ROM are buffered in a queue in an orderly fashion. The resultant flow of μops is next fed to the execution engine.

Front End Branch Predictor:- The branch prediction logic unit predicts the locations from where the next instruction bytes are fetched. The predictions are made on past history of the program execution.

Long type questions [7 marks each]

Q-1) **Explain Micro-architecture of Pentium-4. [S-16(Q5-c)]**
Ans:-It is CPU on a single chip. It

Q-2) **Explain extended instructions set in advanced Pentium processors. [S-16(Q6-c)]**
Ans:-It is CPU on a single chip. It

Q-3) **Explain Pentium 3. [W-17(Q4-c)]**
Ans:-It is CPU on a single chip. It

Q-4) **Give explanation on Instruction Translation Look aside Buffer (ITLB) and Branch prediction. [W-17(Q6-c)]**
Ans:-It is CPU on a single chip

Chapter-VI

(An Introduction to Microcontrollers 8051 & 80196)

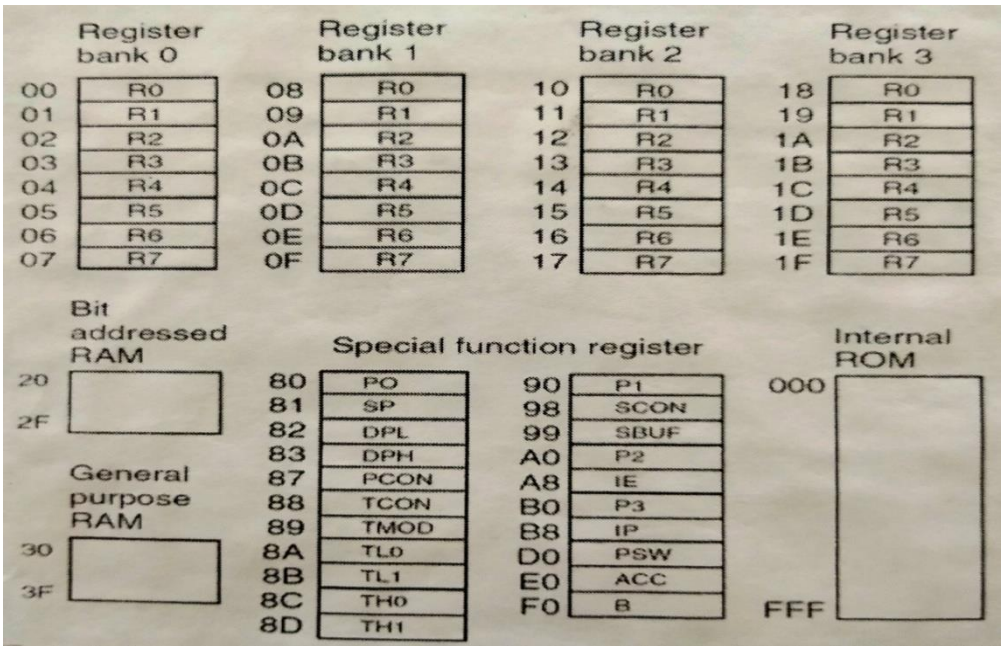
Short type questions [2 marks each]

Q-1)**What is the function of symbol # and @? [S-16(Q7-a)]**
Ans:-The # symbol represents immediate data present in an instruction and the @ symbol represents internal data RAM address addressed indirectly.

Q-2)**What are the interrupts of 8051?. [W-17(Q7-a)]**
Ans:- The 8051 MC has five interrupt signals. They are INT0, TF0, INT1, TF1, RI/TI. Each interrupt can be enabled or disabled by setting its of the IE register.

Medium type questions [5 marks each]

Q-1) **Explain the register sets of 8051 Microcontroller. [S-16(Q7-b)]**
Ans:-



The programming model of 8051 is divided into two major group of registers. Registers that hold data for arithmetic & logical functions are from ALU; and registers called SFRs are from data memory. The programming model includes the working registers(WREG),flag registers (STATUS), file select registers(FSRs), multiplication register, program counter, stack and SFRs.

Working Registers (WREG):- The working register of 8051 is similar to the accumulator in other processor. It is an 8-bit register in ALU that is used in all arithmetic & logic operations. The result of arithmetic or logic operation can be stored in the WREG or in other operand register.

Bank Select Register(BSR):- The BSR is an 8-bit register but uses only the lower 4-bit to specify the data bank from 0 to F and the upper 4-bits are always 0. The data memory has 4096 registers and is divided into 16 banks, each with 256 registers.

STATUS Registers:- The Status register is an 8-bit register that uses 5 individual bits, B_0 to B_4, called flags, reflecting the data conditions of an operation; the remaining 3 bits, B_5 –B_7 are unused. The data condition flags reflect the nature of the result after an

operation. The 5 flags are known as C-carry, DC-digit carry, Z-zero, OV-overflow and N-negative.

File Select Register (BSRs):- There are 3 registers, FSR_0, FSR_1 and FSR_2 hold 12-bit addresses of data registers and are used as pointers for indirect addressing. To hold a 12-bit address FSR, registers require two 8-bit registers- FSRH & FSRL and each FSR register is associated with an INDF register for indirect addressing.

Program Counter(PC):- The PC is a 21-bit register that functions as a counter and provides capability of addressing 2MB of memory. The PC consists of three 8-bit registers- PCL, PCH & PCU. The MC uses this counter to sequence the execution of the instructions.

Table Pointers (TB):- These are 21-bit registers that are used as memory pointers to copy bytes between program memory and data memory.

Stack Pointer (SP):- The stack is a group of 31-word sized registers that are used for temporary storage of memory addresses during the execution of a program. The SP uses 5-bits to indicate where the instructions that are used to store and retrieve information from the 31 register stack.

Special Function Register(SFR):- In programming model, 10 blocks are shown as special function registers representing register associated with the I/O ports, support devices and process of data transfer. The SFRs associated with various devices in the MCU are I/O port, Interrupt, EERPROM, Serial I/O, Timers, CCP register, A/D converter, Synchronous serial I/O and other registers.

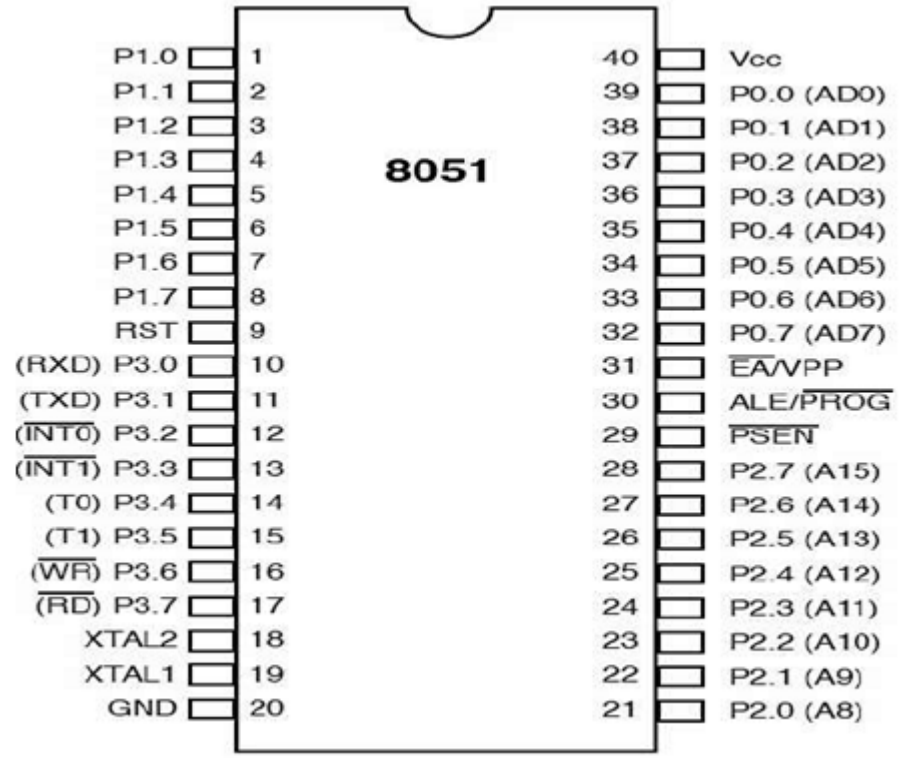
Q-2) **Design a Microcontroller 8051 based length measurement system for continuously rolling cloth or paper. [S-17(Q7-b)]**

Ans:-It is CPU on a single chip

Long type questions [7 marks each]

Q-1) **Draw the signal description of 8051 and explain the function of each pin.**
[S-16(Q7-c)], [W-17(Q7-b)], [S-17(Q6-c)], [S-19(Q6-c)]

Ans:- The pin diagram of 8051 is shown below-

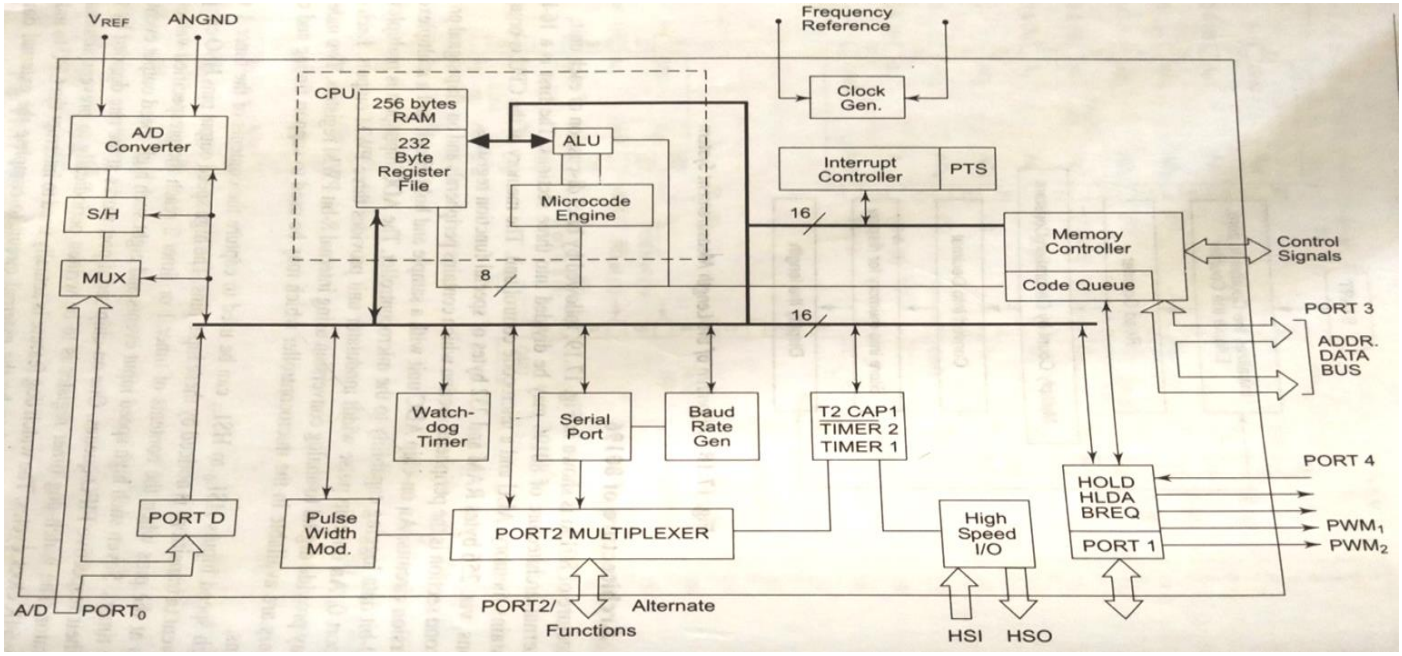


V_{cc}(Pin-40):- It is a +5V supply voltage pin.
GND(Pin-20):- It is the return pin for the power supply.
RESET(Pin-9):- The reset pin resets the 8051, only when it goes high for two or more machine cycles.
ALE/$\overline{PROG}$(Pin-30):- The address latch enable(ALE) o/p pulse indicates that the valid address bits are available on their respective pins. The ALE signal is valid only for external memory access.
$\overline{PSEN}$(Pin-29):- It is program strobe enable. It is o/p control signal which a read strobe to external program memory. This goes low during external program memory access.
$\overline{EA}$/V_{PP}(Pin-31):- It is external access. It controls the access of program of program memory. The 8051 can execute a program in external memory, only if $\overline{EA}$ is tied low. For execution of program in internal memory, the $\overline{EA}$ is tied high.
XTAL1(Pin-19):- It is i/p to the inverting amplifier which is a part of the on chip oscillator ckt. When external clock is used, it is connected to the external oscillator signal.
XTAL2(Pin-18):- It is o/p to the inverting amplifier which is a part of the on chip oscillator ckt. When external clock is used, it is left unconnected to the external oscillator signal.
PORT 0(Pin-32 to 39):- Port 0 is an 8-bit bidirectional bit addressable I/O port. This has been allotted an address in the SFR address range. Port 0 acts as multiplexed address/data lines during external memory access(i.e) when $\overline{EA}$ is low and ALE emits a valid signal. In case of controllers with on chip EPROM, Port 0 receives code bytes during programming of the internal EPROM.
PORT 1(Pin-1 to 8):- Port 1 acts as a 8-bit bidirectional bit addressable port. This has been allotted an address in the SFR address range.
PORT 2(Pin-21 to 28):- Port 2 acts as a 8-bit bidirectional bit addressable I/O port. This has been allotted an address in the SFR address range. During external memory accesses, port2 emits higher 8-bit of address(A_8 –A_{15}) which are valid, if ALE goes high and $\overline{EA}$ is low. Port2 also receives higher order address bits during programming of the on chip EPROM.

PORT 3(Pin-10 to 17):- Port 3 is an 8-bit bidirectional bit addressable I/O port. This has been allotted an address in the SFR address range. The port3 also serve the alternative functions as follows-
P3.0- Acts as serial input data pin (RxD)
P3.1- Acts as serial output data pin (TxD)
P3.2- Acts as external interrupt pin 0 ($\overline{INT0}$)
P3.3- Acts as external interrupt pin 1 ($\overline{INT1}$)
P3.4- Acts as external input or timer-0 (T0)
P3.5- Acts as external input or timer-1 (T1)
P3.6- Acts as write control signal for external data memory ($\overline{WR}$)
P3.7- Acts as read control signal for external data memory ($\overline{RD}$)

Q-2) **Explain 16-bit Microcontroller family MCS-96 with neat block diagram. [S-17(Q7-c)]**

Ans:- The MCS-96 family of microcontroller caters the needs of applications in the field of closed loop control, modems, printers, disk drives and medical instrumentation. 80196 is a member of MCS-96 microcontroller family.



The internal architecture is divided into 3 sections.

The first is a 16-bit CPU which contains memory, ALU and a microcode control unit. The memory of the CPU is organised in two sections- 256 bytes RAM and 232 bytes of SFRs.

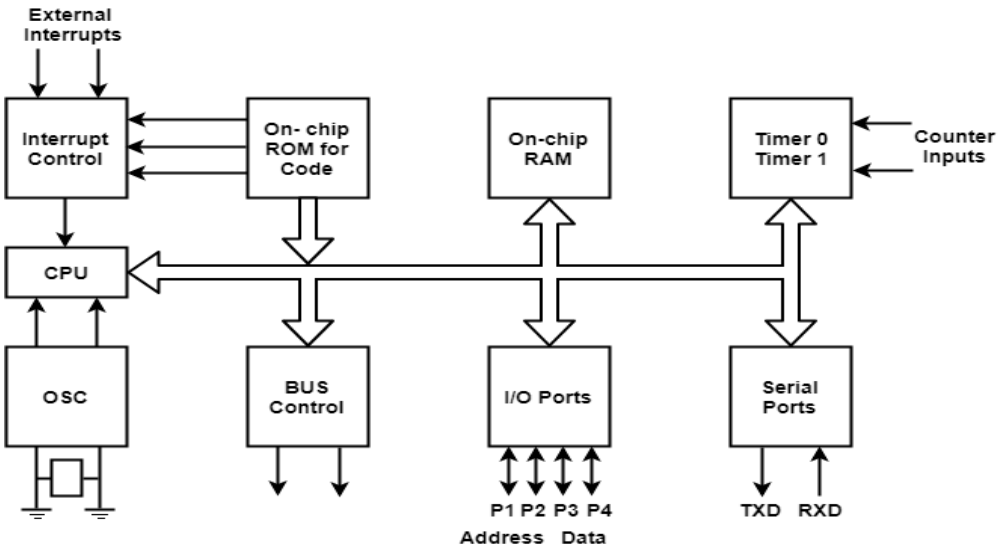
The second section is the peripheral sections which contains peripherals and on chip signal processing and conversion circuits. An on chip ADC unit with a sample and hold ckt and a multiplexer offers 8-bit or 10-bit data logging capability to the microcontroller. The ADC input port is multiplexed with 8-bit I/O port 0. An on chip pulse width modulation unit provides three PWM outputs which may provide digital to analog conversion using internal 8-bit PWM registers. Two independent 16-bit timers are available in the microcontroller which may be used to support timing and counting applications.

The third section consists of bus control circuits. The bus control ckt unit consists of a memory controller which controls the external memory access and fetches the instructions for execution. The fetched instructions are arranged in a queue. The opcodes from the queue are further sent to the microcode control unit over an internal 8-bit bus, while the data may be sent over the internal 16-bit bus, if required for execution. The bus hold section, handles the bus requests from other masters, in case of multimaster systems. The clock generator generates

basic system timings using a crystal of 16 MHz frequency. The ALU of 80196 is called Register Arithmatic Logic Unit(RALU)& it is integrated with the special function register bank.

Q-3) **Describe the architecture of 8051. [W-17(Q7-c)]**

Ans:- A microcontroller architecture consists of a CPU, two kinds of memories, I/O ports, the mode status, data registers and random logic needed for a variety of peripheral functions.



CPU:- MCS-51/8051 consists of 8-bit ALU with associated registers like A,B,PSW,SP,the 16-bit PC and DPTR register. The ALU perform arithmatic and logic operation on 8-bit operand.

BOOLEAN PROCESSOR:- There is a separate boolean processor integrated within the 8051 MC. It has own instruction sets, accumulators and bit address level RAM.It allowes bit manupulation perform operation line, comliment bit, set bit, clear bit.

REGISTERS:- There are special function registers(SFR) which are the prgoram status word, accumulator, register, stack pointer, register for serial I/O ports, interrupt handlers.

PROGRAM & DATA MEMORY:- There are two separate program and data memory. The code is stored in ROM/EPROM. RAM of 8051 MC is 1128 bytes. RAM is used for controlling the operation of the peripheral timer/counter serial ports interrupt etc.

PORTS(P0,P1,P2,P3):- 8051 MC has four ports P_0,P_1,P_2 & P_3 each port is 8-bit in single chip made. There are two timer and serial interface(SI).

OSCILLATOR:- The 8051 MC used and external crystal oscillator function. The frequency of operation can be depending upon the individual device data sheets of the device can be reffered to see the operating fequency supported by typical device.

Q-4) **With proper example explain the addressing modes of 8051. [S-19(Q3-c)]**

Ans:- The addressing modes of Intel 8051 are-

Register addressing, Direct addressing, Register Indirect addressing, Immediate addressing and Bas register plus Index register Indirect addressing.

Register addressing:- The 8 working registers of the selected register bank are accessed by register addressing. The last significant 3-bits of

the instruction Op-code indicate which register is to be accessed. ACC, B, DPTR and CY are also accessed by register addressing.

Direct addressing:- The only method to access SFRs is direct addressing. The lower 128 bytes of internal RAM are also accessed by this addressing.

Register-Indirect addressing:- The content of either R0 and R1 is used as a pointer to access memory locations in the 256 bytes block; the lower 128 bytes of internal RAM, the upper 128 bytes of internal RAM and the lower 256 bytes of external data memory. SFRs are not accessible by register-indirect addressing. Full 64K of external data memory are accessed by 16-bit DPTR. This addressing is also useful for the execution of PUSH or POP instruction. The SP may reside anywhere in the internal RAM.

Base Register plus Index-Register Indirect addressing:- It is used to access a byte from the location whose address is the sum of a base register (DPTR or PC) and an index register. Acc is used as index register. This mode is used look up table access. Program memory address @DPTR+A or @PC+A.