CHAPTER-1

2 marks questions

<u>1.Convert the decimal no.$(1000)_{10}$ into binary</u> [2016]

2	1000	
2	500	0
2	250	0
2	125	0
2	62	1
2	31	0
2	15	1
2	7	1
2	3	1
	1	1

Ans.$(1111101000)_2$

<u>2.Convert (10110101) from binary to gray code</u>[2016]

1 0 1 1 0 1 0 1 (binary)
↓
1 1 1 0 1 1 1 1 (gray)

<u>3. Perform 2's complement substraction of 1000011-1010111</u>[2014,2016]

$(67)_{10} - (87)_{10} = (-20)_{10}$

Convert substrate part into 2's complement

$$1010111 \xrightarrow{1's} \begin{array}{r} 0101000 \\ +\quad 1 \\ \hline 0101001 \end{array} \Big\downarrow \text{ 2's comp}$$

Then add both manuent and substrant

```
     1000011
+    0101001
-----------
     1101100
```

Here there is no carry ,if there is no carry then substrate 1 from the result then recomplement it.

```
     1101100
-          1
-----------
     1101011
```

Then recomplement of this $(0010100)_{10}$

4.What is the difference between weighted and non weighted binary code [2016]

- The weighted codes are those that obey the position weighting principle ,which states that the position of each number represent a specific weight .
- The non-weighted codes are not positionally weighted .In other words codes that are not assigned with any weight to each digit position.

5.Convert the binary no.$(10110111.1101)_2$ to decimal[2015]

$(10110111.1101)_2$

$1\times2^{7}+1\times2^{5}+1\times2^{4}+1\times2^{2}+1\times2^{1}+1\times2^{0}+1\times2^{-1}+1\times2^{-2}+1\times2^{-4}$

128+32+16+4+2+1+1/2+1/4+1/16

183.81

6.What are the application of gray code[2015]

- Used as counter
- Used for asynchronous fifo’s adress pointer
- Help to reduce the digital noise
- High speed decode circuit
- Also use in computers to address program memory .

7.What is parity bit[2015]

It is an error detection scheme used to detect a change in the value of a bits (0 or 1) during transmission to detect error .

8.What is the base or radix of a number system[2013]

The Radix of a number system is defined as the number of different digits which can occur in each position in the number system for example :Decimal number system has a base or radix of 10

9.Convert $FADE_{16}$ to binary and octal[2013]

In the binary form

FADE is $(1111\ \ 1010\ \ 1101\ \ 1110)_2$

In octal form

001 111 101 011 011 110

1 7 5 3 3 6

Answer is $(175336)_8$

10.Convert 7743_g to binary and hexadecimal.[2013]

For binary

7 7 4 3

111 111 100 011

In the binary form the answer is $(111\ \ 111\ \ 100\ \ 011)_2$

For hexadecimal

First octal is converted to binary then to hexadecimal .

7 7 4 3

111 111 100 011

15 14 3

In the hexadecimal form the answer is $(FE3)_{16}$

11.<u>Which code is known as self correcting code and why</u> ?[2017]

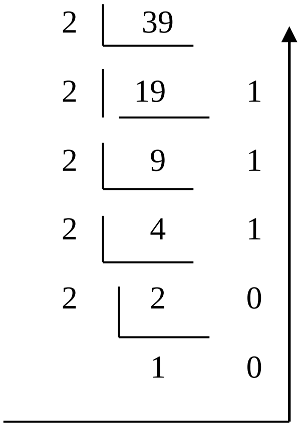
Error correcting code is known as self correcting code because this code is enough to detect one bit error as well as correct the error .

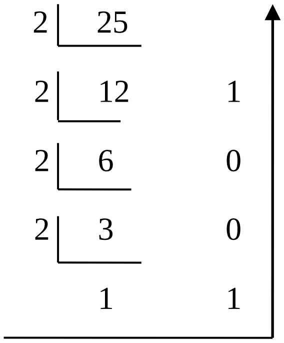
5 marks questions

1.<u>What are the difference between 1's complement and 2's complement ?Substrat $(39)_{10}$ and $(25)_{10}$ using 2's complement</u>[2015]

1's complement of a binary number can be find out by complementing 1 to 0 and 0 to 1 means (in place of 0 we put 1 and in place of 1 we put 0)

2's complement of the number can be findout by adding 1 to the 1's complement of the given number . 39-25=?





$(100111)_2$ $(11001)_2$

Convert equal bi39--------------100111

25--------------011001

Convert substrant into 2's complement

011001------------100110

$$\begin{array}{r} 100110 \\ + \quad 1 \\ \hline 100111 \end{array}$$

Then add both

100111

100111

~~1~~001110

Ans. 001110

7 marks questions

1.<u>Explain ASCII code and its application and distinguish between weighted and non weighted code</u>[2015]

The code is known as American standard code for information interchange and written as ASCII and pronounced as “as kee” was developed as orderly binary code applicable to alphanumeric data .

This code is used for printers and teletype writers .In weighted code for each position or bit there is specific weight attached .It is used in binary system .

Suitable example –

A binary number=11110

Here the weighted codes are two and the weighted codes are written as

1	1	1	1	0
2^4	2^3	2^2	2^1	2^0

Similarly in unweighted codes there is no specific weight attached .

Chapter 2

2 marks Questions

1. <u>Write down the truth table of 2 input ex-or gate</u>[2014]

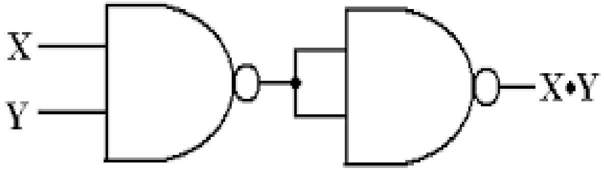
A	B	Y=A+B
0	0	0
0	1	1
1	0	1
1	1	0

5 marks questions

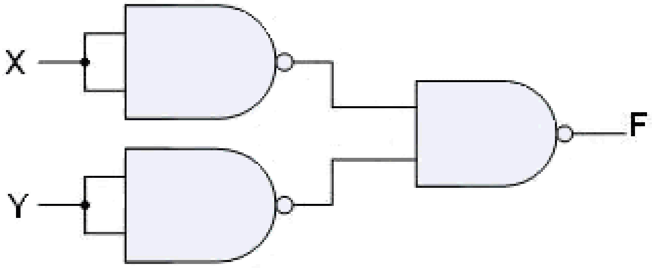
1.Which gates are referred to as universal gates and why ?How other gates can be realized using NAND gates[2014, 2015,2016,2017]

NAND gate and NOR gate are known as universal logic gates .All logic gates are implemented using NAND and NOR gate only.

AND gate using NAND gate

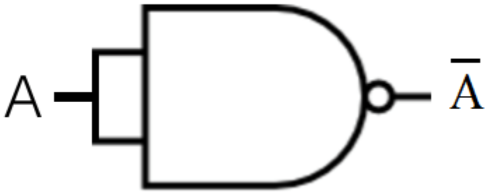


OR gate using NAND gate

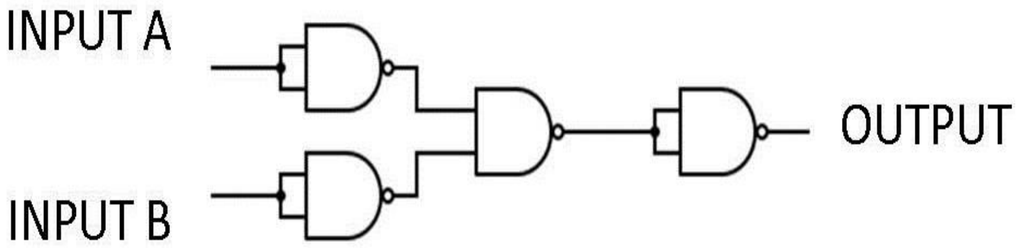


OR using NAND

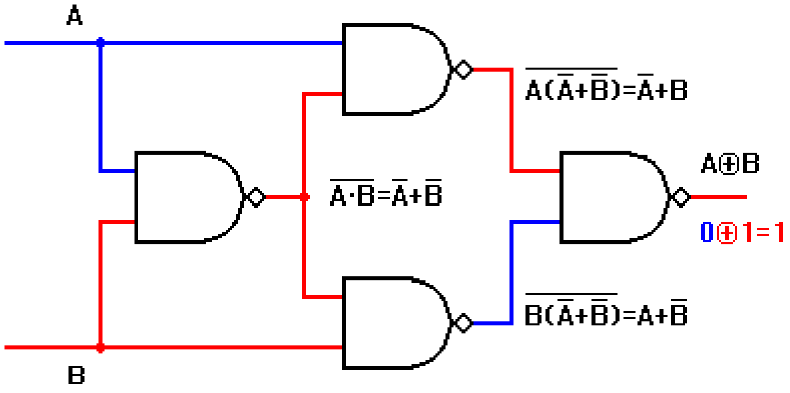
NOT gate using NAND gate



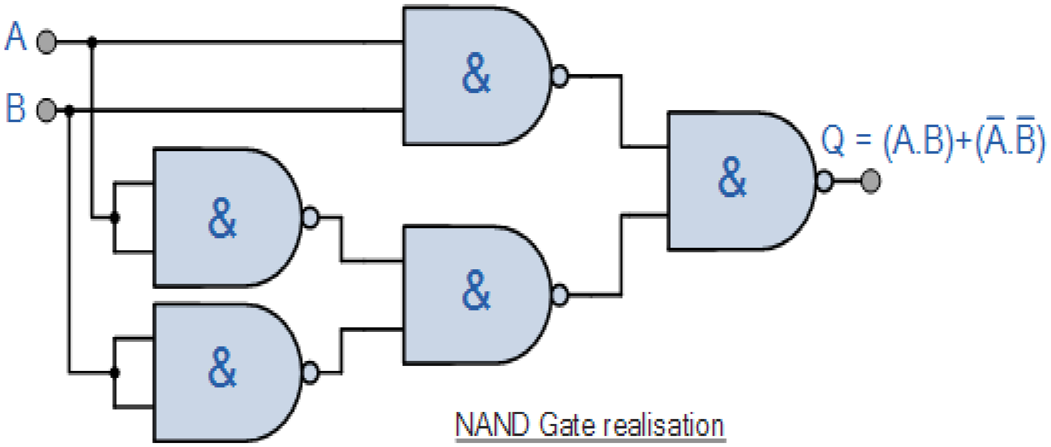
NOR gate using NAND gate



EX-OR gate using NAND gate

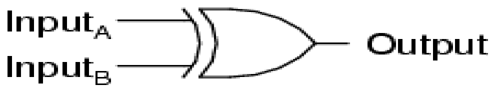


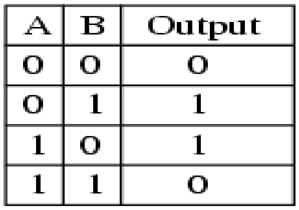
EX-NOR gate using NAND gate



2.<u>Draw the symbol ,truth table and expression for</u> <u>x-or</u> **<u>and AND gates</u>[2015]**

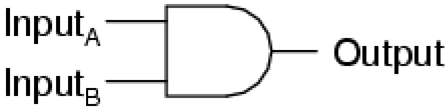
Exclusive-OR gate

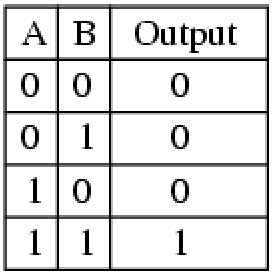




A	B	Output
0	0	0
0	1	1
1	0	1
1	1	0

2-input AND gate





A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1

7 marks questions

1. <u>What is universal gate ? explain with examples and realise other gate</u>[2015]

Same as 5 marks question no.1

Chapter 3

2 marks Questions

1.Define demorgan's law[2014 , 2015,2017]

- This law states that the complement of any expression can be obtained by replacing each variable and element with its complement and changing OR operators with AND operators and AND operators to OR operators .These can be expressed

  A) $\overline{X + Y} = \overline{X} \,.\, \overline{Y}$

  B) $\overline{X \,.\, Y} = \overline{X} + \overline{Y}$

2.Define racing conditation[2014 ,2016 , ,2017]

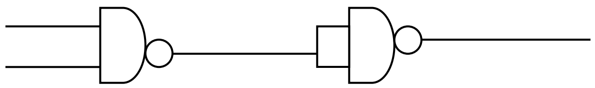
A race condition is an undesirable situation that occurs when a device or system attempts to perform 2 or more operations at the same time ,but because of the nature of the device or system, the operation must be done in the proper sequence to be done correctly

5 marks Questions

1.Simplify the Boolean expression a[b+c($\overline{ab+ac}$)] [2016]

$A[b+c(\overline{ab+ac})] = a[b+c(\overline{ab} \times \overline{ac})] = a[b+c(\overline{a}+\overline{b})(\overline{a}+\overline{c}) = a[b+c(\overline{a}\times\overline{a} + \overline{a}\times\overline{b} + \overline{a}\times\overline{c} + \overline{b}\times\overline{c})]$

$a[b+c(\overline{a} + \overline{a}\ \overline{b} + \overline{a}\ \overline{c} + \overline{b}\ \overline{c})] = a[b + c\overline{a}(1 + \overline{b} + \overline{c}) + \overline{b}\ \overline{c}\ c] = a[b + \overline{a}\ c] = ab$



2.Simplify the expression[2015]

$$Y = \overline{(AB+\overline{C})(\overline{A+b+C})}$$

$\overline{(AB+\overline{C})} + \overline{(\overline{A+B}+C)} \qquad = [\overline{AB} \times \overline{\overline{C}}\,] + \{\overline{\overline{A+B}}\} \times \overline{C}$

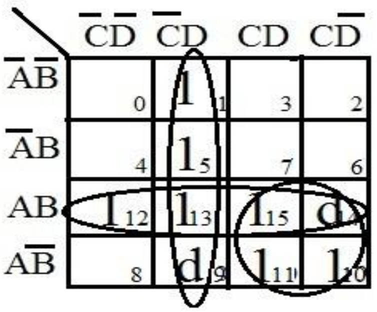
$= [\overline{AB} \times C] + (A+B) \times \overline{C}$

$= [(\overline{A}+\overline{B})C] + (A+B) \times \overline{C}$

$= \overline{A}C + \overline{B}C + A\overline{C} + B\overline{C}$

3.<u>Simplify the following expression using k-map</u>[2015]

Y(A ,B ,C ,D)=∑(1 ,5 ,10 ,11 ,12 ,13 ,15) +D(9 ,14)



	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	$_{0}$	1_{1}	$_{3}$	$_{2}$
$\overline{A}B$	$_{4}$	1_{5}	$_{7}$	$_{6}$
AB	1_{12}	1_{13}	1_{15}	d
$A\overline{B}$	$_{8}$	d_{9}	1_{11}	1_{10}

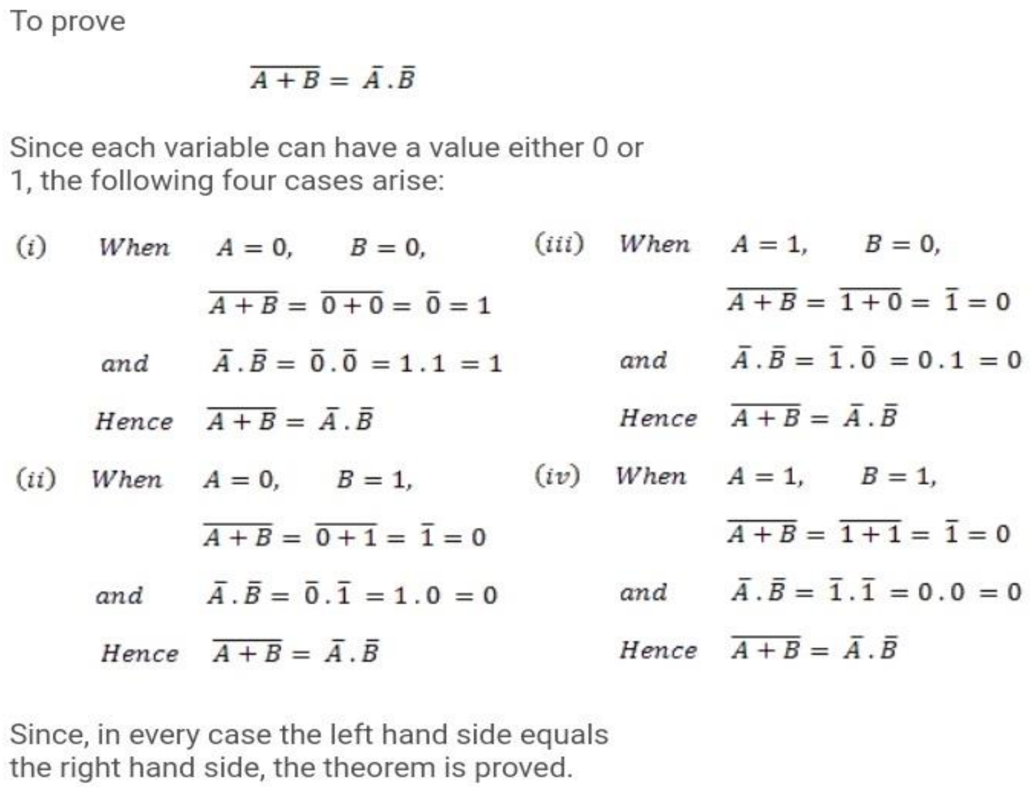
$AB+\overline{C}D+AC$

4.<u>State and prove demorgan's theorem</u> [2013]

This theorem states that the complement of any expression can be obtained by replacing each variable and the operators of or is changed to AND and via-versa.

$\overline{X + Y} = \overline{X} \,.\, \overline{Y}$

$\overline{X \,.\, Y} = \overline{X} + \overline{Y}$



To prove

$$\overline{A+B} = \bar{A}.\bar{B}$$

Since each variable can have a value either 0 or 1, the following four cases arise:

(i) *When* $A = 0,\quad B = 0,$

$\overline{A+B} = \overline{0+0} = \bar{0} = 1$

and $\bar{A}.\bar{B} = \bar{0}.\bar{0} = 1.1 = 1$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

(ii) *When* $A = 0,\quad B = 1,$

$\overline{A+B} = \overline{0+1} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{0}.\bar{1} = 1.0 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

(iii) *When* $A = 1,\quad B = 0,$

$\overline{A+B} = \overline{1+0} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{1}.\bar{0} = 0.1 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

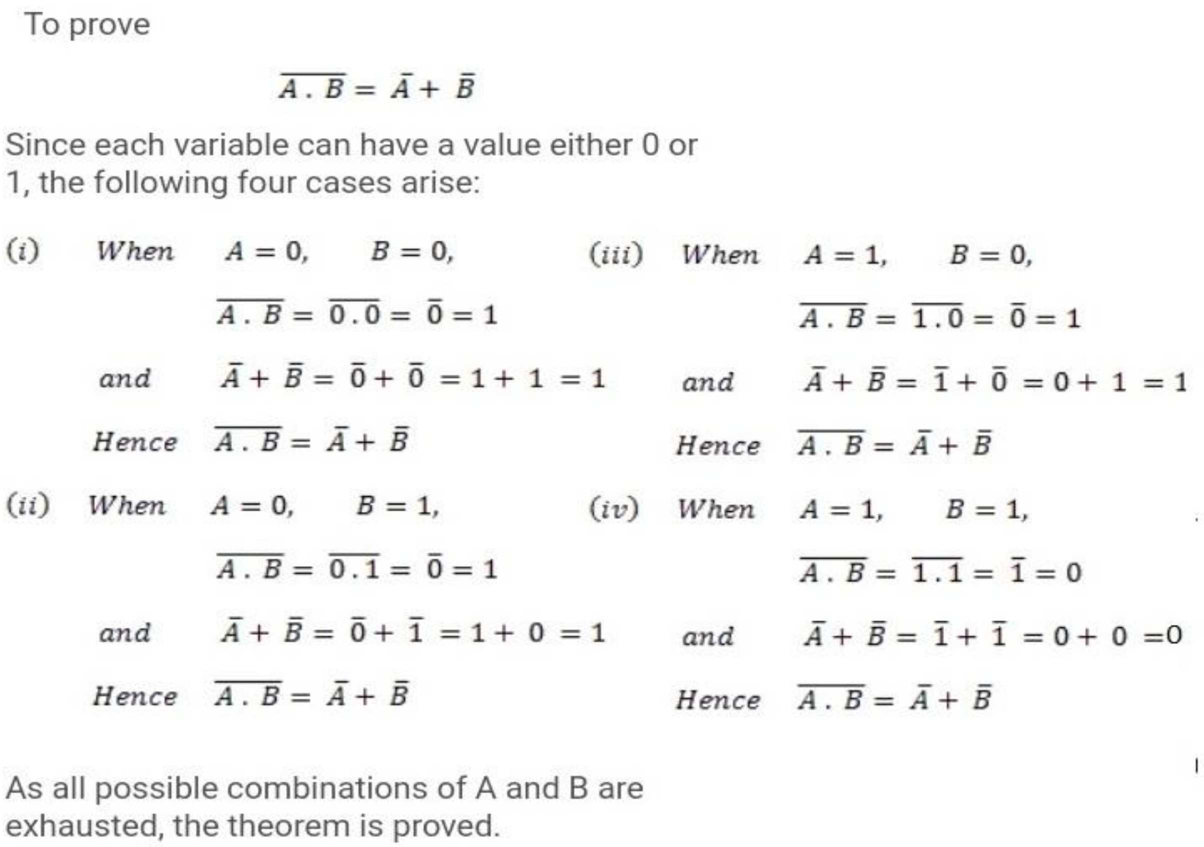
(iv) *When* $A = 1,\quad B = 1,$

$\overline{A+B} = \overline{1+1} = \bar{1} = 0$

and $\bar{A}.\bar{B} = \bar{1}.\bar{1} = 0.0 = 0$

Hence $\overline{A+B} = \bar{A}.\bar{B}$

Since, in every case the left hand side equals the right hand side, the theorem is proved.



To prove

$$\overline{A\,.\,B} = \bar{A} + \bar{B}$$

Since each variable can have a value either 0 or 1, the following four cases arise:

(i) *When* $A = 0, \quad B = 0,$

$\overline{A\,.\,B} = \overline{0\,.\,0} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{0} + \bar{0} = 1 + 1 = 1$

Hence $\overline{A\,.\,B} = \bar{A} + \bar{B}$

(ii) *When* $A = 0, \quad B = 1,$

$\overline{A\,.\,B} = \overline{0\,.\,1} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{0} + \bar{1} = 1 + 0 = 1$

Hence $\overline{A\,.\,B} = \bar{A} + \bar{B}$

(iii) *When* $A = 1, \quad B = 0,$

$\overline{A\,.\,B} = \overline{1\,.\,0} = \bar{0} = 1$

and $\bar{A} + \bar{B} = \bar{1} + \bar{0} = 0 + 1 = 1$

Hence $\overline{A\,.\,B} = \bar{A} + \bar{B}$

(iv) *When* $A = 1, \quad B = 1,$

$\overline{A\,.\,B} = \overline{1\,.\,1} = \bar{1} = 0$

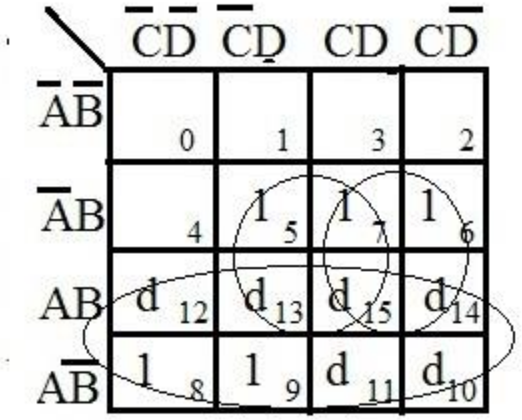
and $\bar{A} + \bar{B} = \bar{1} + \bar{1} = 0 + 0 = 0$

Hence $\overline{A\,.\,B} = \bar{A} + \bar{B}$

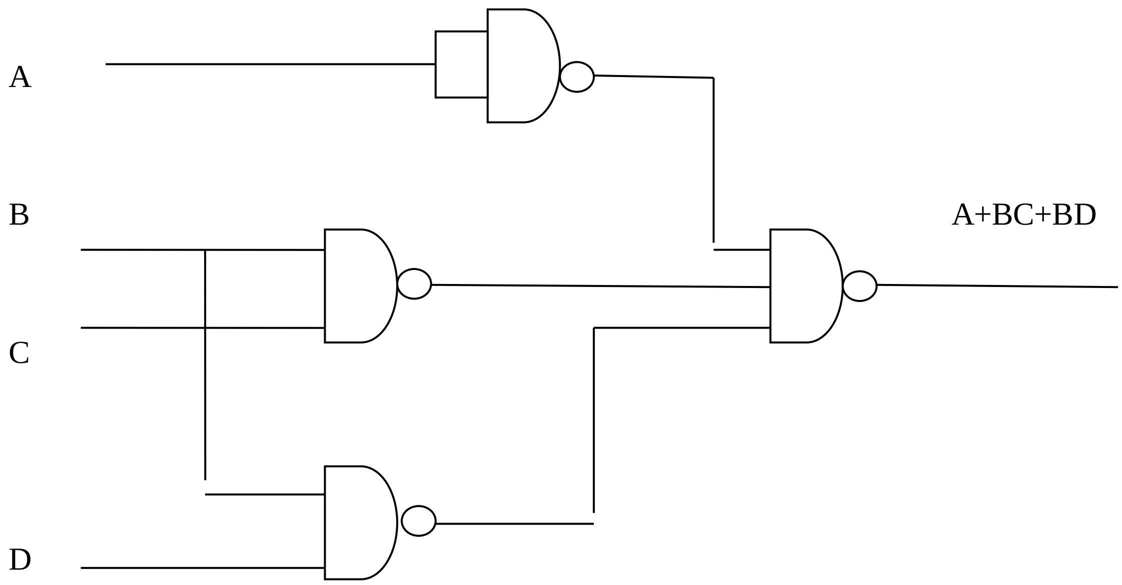
As all possible combinations of A and B are exhausted, the theorem is proved.

7 marks Questions

1.Simplify the given expression using k-map and draw the logic circuit using NAND gate only. F(a ,b ,c ,d)=$\sum_m$ (5 ,6 ,7 ,8 ,9)+d(10 ,11 ,12 ,13 ,14 ,15) [2016]



	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	0	1	3	2
$\bar{A}B$	4	1 5	1 7	1 6
AB	d 12	d 13	d 15	d 14
$A\bar{B}$	1 8	1 9	d 11	d 10



2.**Define sop and pos term .Obtain the canonical sop form of the function . Y(A ,B ,C)=A+BC and draw the truth table**[2015]

Sop :- When the product terms goes for logical OR operation OR operation then the final expression is in sum of product expression or sop form .
Ex: $AB + A\overline{B}C + ABC$

Pos :- When two or more sum terms goes for logical AND operation then the output of the AND gate is in pos form .

Ex $(A+\overline{B})(\overline{A}+\overline{B}+C)$

$Y(A,B,C)=A+\overline{B}\overline{C}=A(B+\overline{B})(C+\overline{C})+\overline{B}\overline{C}(A+\overline{A})$

$=(AB+A\overline{B})(C+\overline{C})+A\overline{B}\overline{C}+\overline{A}\,\overline{B}\,\overline{C}$

$=AB(C+\overline{C})+A\overline{B}(C+\overline{C})+\overline{AB}\overline{C}+\overline{A}\,\overline{B}\;\overline{C}$

$=ABC+A\overline{BC}+\overline{A}BC+\overline{A}B\overline{C}+\overline{AB}\overline{C}+\overline{A}\,\overline{B}\,\overline{C}$

$=M_7+M_6+M_5+M_4+\cancel{M_4}+M_0$

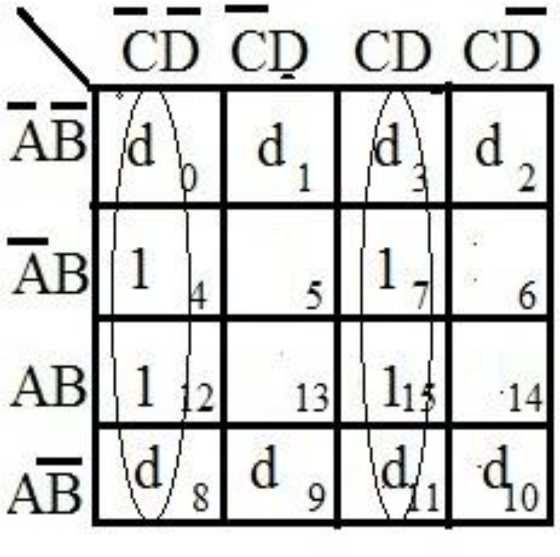
$=M_0+M_4+M_5+M_6+M_7$

$=\sum_m(0,4,5,6,7)$

Truth table :-

A	B	C	F
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

3.**Simplify the expression by using k-mapF(A ,B,C,D)=$\sum_{M}$(4 ,7 ,12 ,15)+D(0 ,1 ,2 ,3,8 ,9 ,10 ,11) and implement it with NAND gete.[2014]**



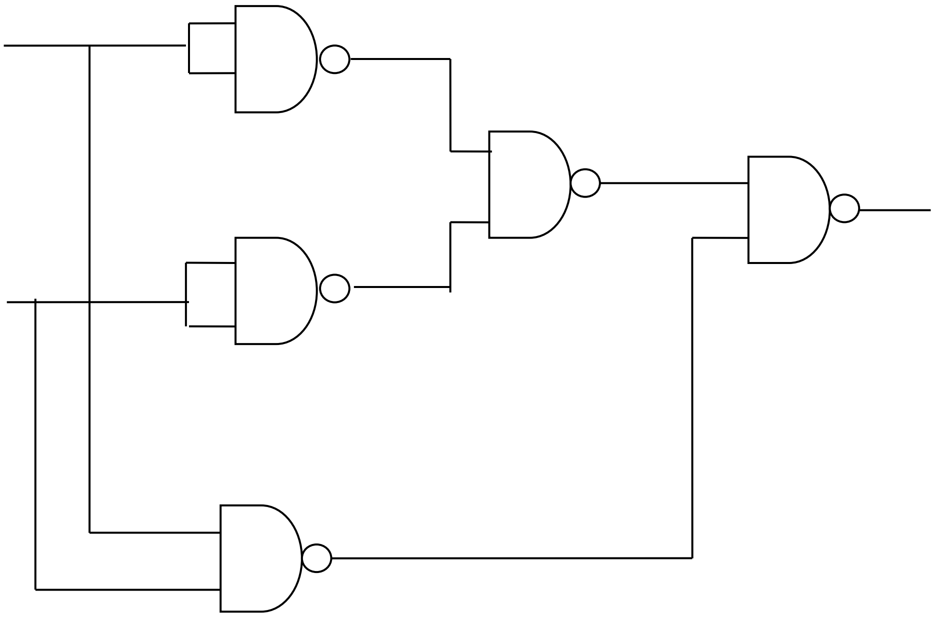
	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	d 0	d 1	d 3	d 2
$\overline{A}B$	1 4	5	1 7	6
AB	1 12	13	1 15	14
$A\overline{B}$	d 8	d 9	d 11	d 10

In loop 1 we get $\overline{C}\ \overline{D}$

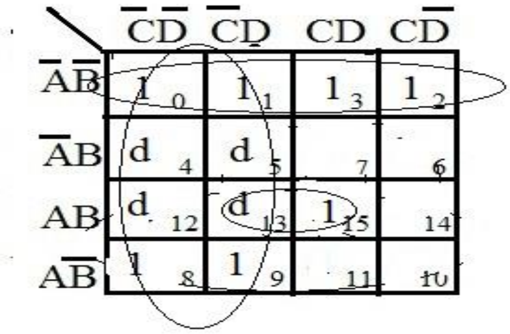
In loop 2 we get C D

output (F) = $\overline{C}\ \overline{D}$

Implementation nand gate design

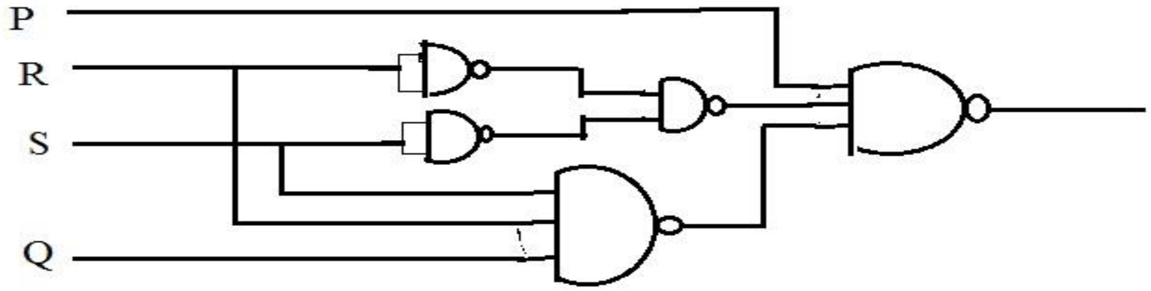


4.<u>Simplify and minimize the 4 variable logic expression F(P ,Q ,R ,S)=Σ(0 ,2 ,4 ,6 ,8 ,12 ,15)+D(1 ,3 ,5 ,7) by using k-map and implement this ircuit by using NAND gate</u> .[2017]



	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1_{0}	1_{1}	1_{3}	1_{2}
$\overline{A}B$	d_{4}	d_{5}	$_{7}$	$_{6}$
AB	d_{12}	d_{13}	1_{15}	$_{14}$
$A\overline{B}$	1_{8}	1_{9}	$_{11}$	$_{10}$

$\overline{P}+\overline{R}\,\overline{S}+QRS$



Chapter 4

2 marks Questions

1.<u>What is an encoder and where it is used</u> [2014]

An encoder is a device whose inputs are decimal digits and outputs are coded representation of input .It has 2^n inputs and 1 output .It has n of control signal .

2.<u>Why multiplexers are referred to as data selectors ?</u>[2017]

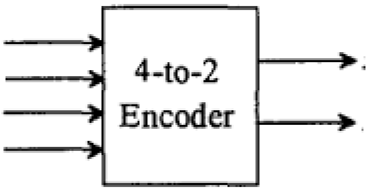
Multiplexer is a combinational logic circuit which have many input but only one output .So it is used as a data selector .

5 marks Questions

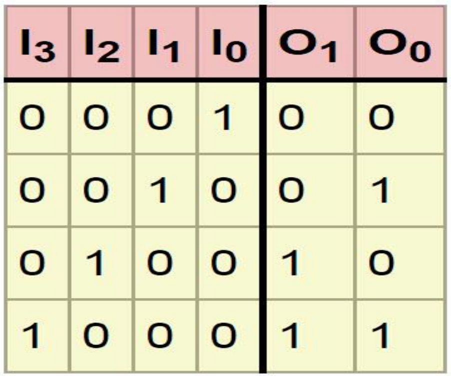
1. <u>Design a 4:2 encoder with neat circuit diagram</u>.[2016,2017]

Input $=2^n=4=$input

N=output
Input----------I_0 ,I_1 ,I_2,I_3
Output--------D_0 ,D_1

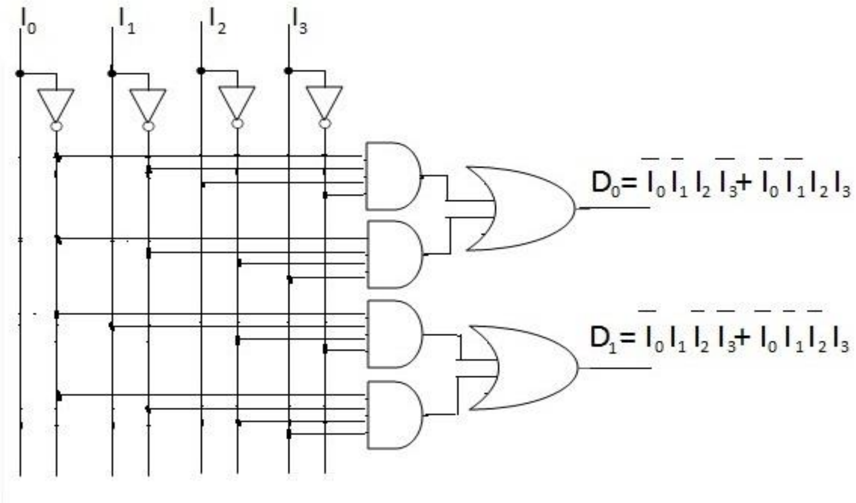


Truth table :-

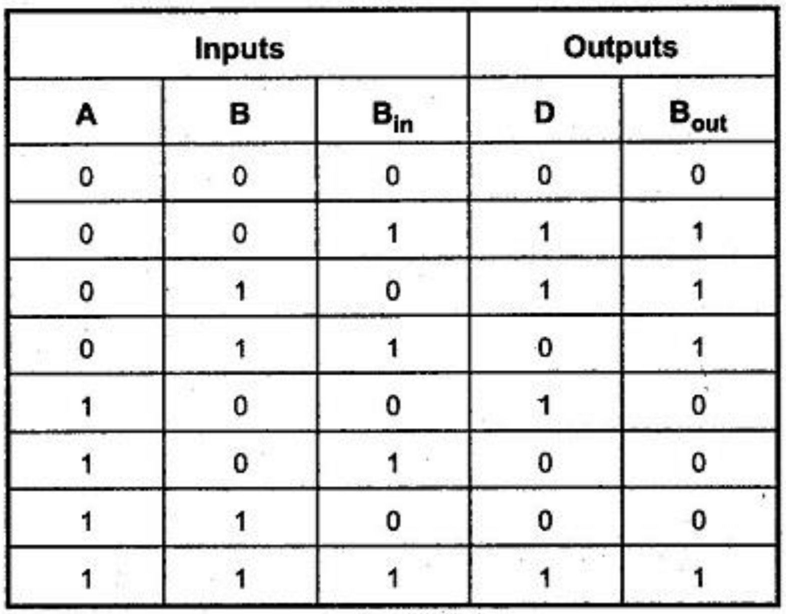


I_3	I_2	I_1	I_0	O_1	O_0
0	0	0	1	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	0	1	1

Logic diagram :-

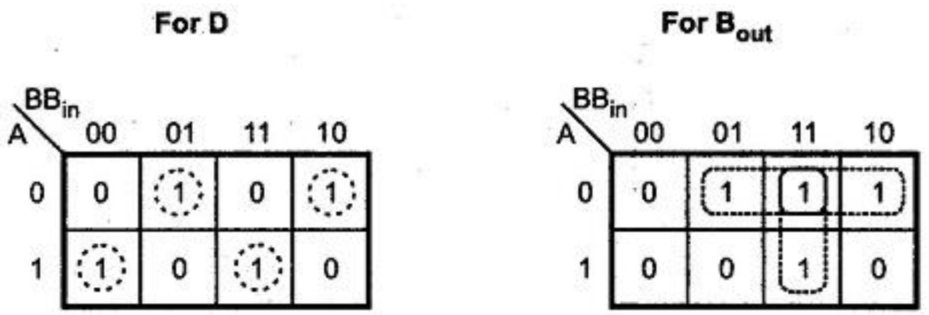

I_0
I_1
I_2
I_3
$D_0 = \bar{I}_0 \bar{I}_1 I_2 \bar{I}_3 + \bar{I}_0 \bar{I}_1 I_2 I_3$
$D_1 = \bar{I}_0 I_1 \bar{I}_2 \bar{I}_3 + \bar{I}_0 \bar{I}_1 \bar{I}_2 I_3$

2.<u>Describe the operation of full substractors with the help of truth table and circuit diagram</u>[2013 ,2014,2016 ,2017]



Inputs			Outputs	
A	B	B_{in}	D	B_{out}
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

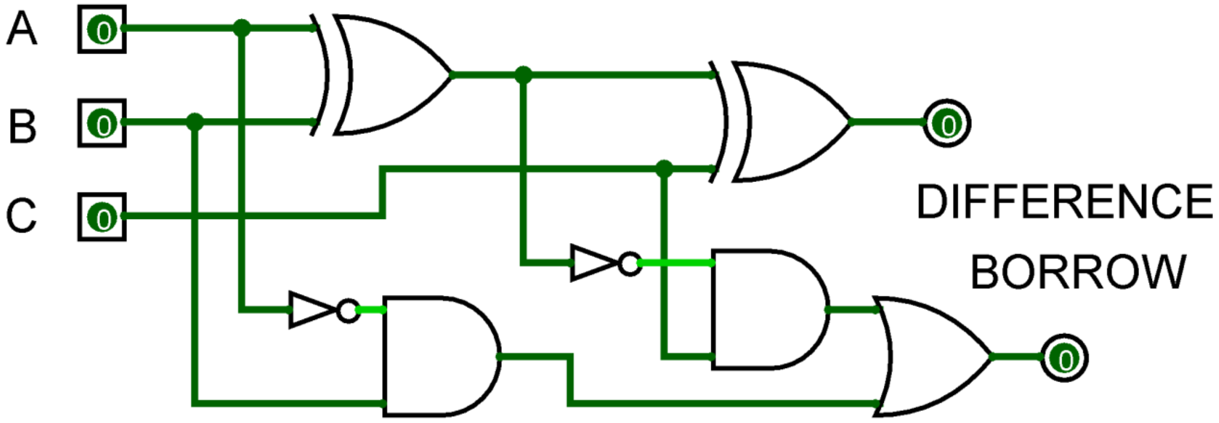
Table 3.9 Truth table for full-subtractor



$D = \overline{A}\overline{B}B_{in} + \overline{A}B\overline{B}_{in} + A\overline{B}\overline{B}_{in} + ABB_{in}$

$B_{out} = \overline{A}B_{in} + \overline{A}B + BB_{in}$

Fig. 3.21 Maps for full-subtractor



7 marks questions

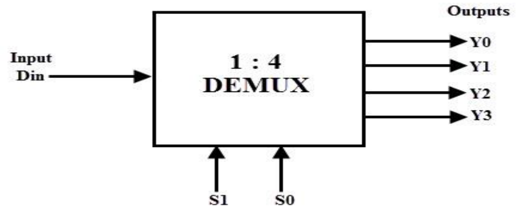
1. <u>With neat circuit diagram explain the function of 1:4 de-mux & 4:1 mux.</u>[2015 ,2017]

1:4 DEMUX

No. of input =1

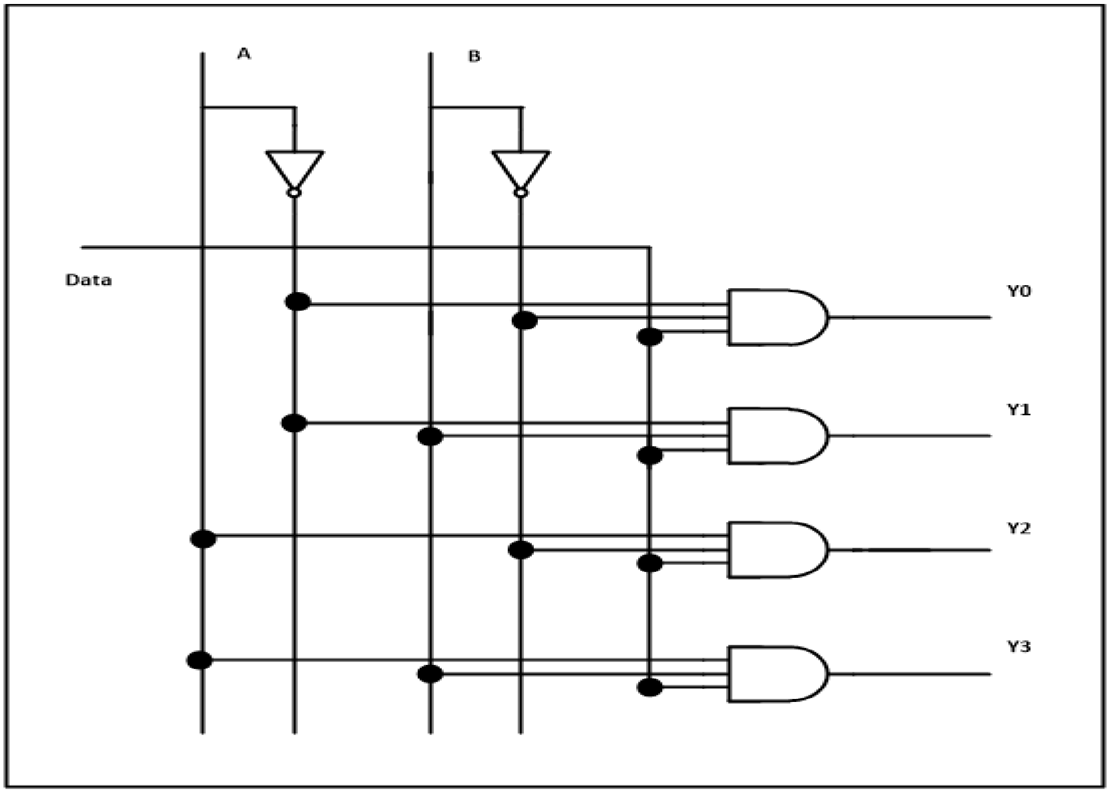
No. 0f selection line =n=2

No. of output =2^2=4



Input	Select Lines	Output Lines
I	S_1 S_0	$Y_0 Y_1 Y_2$ Y_3
I	0 0	1 0 0 0
I	0 1	0 1 0 0
I	1 0	0 0 1 0
I	1 1	0 0 0 1

$Y_0 = \overline{S}_0 \overline{S}_1 I$,$Y = S_0 \overline{S}_1 I$,$Y = \overline{S}_0 S_1 I$,$Y = S_0 S_1 I$



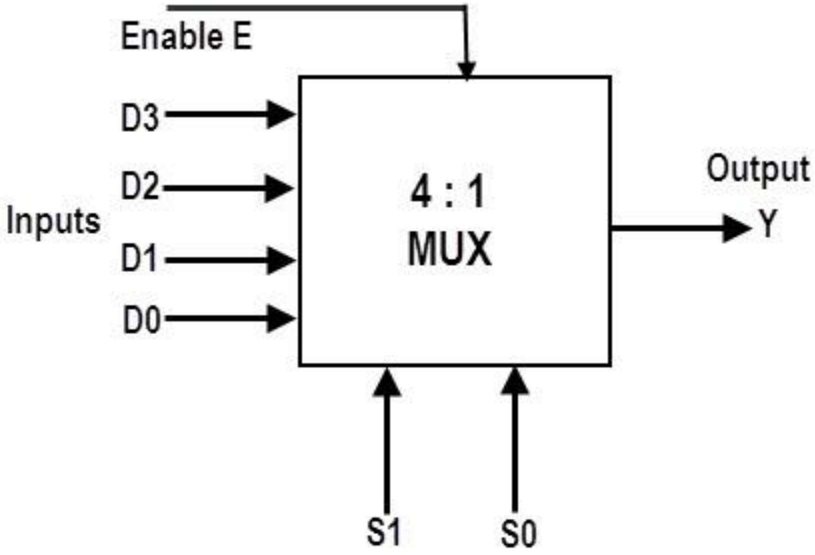
4:1 MUX

4:1 MUX = 2^n :1 =2^2 :1mux

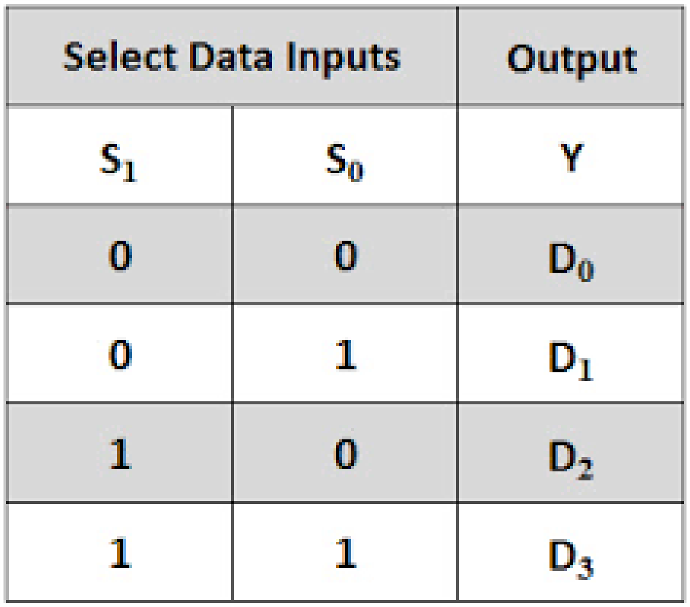
No. of inputs =2 =4(D_0 D_1 D_2 D_3)

No. of selection line =n =2(S_1 , S_0)

No. of output =1 (Y)

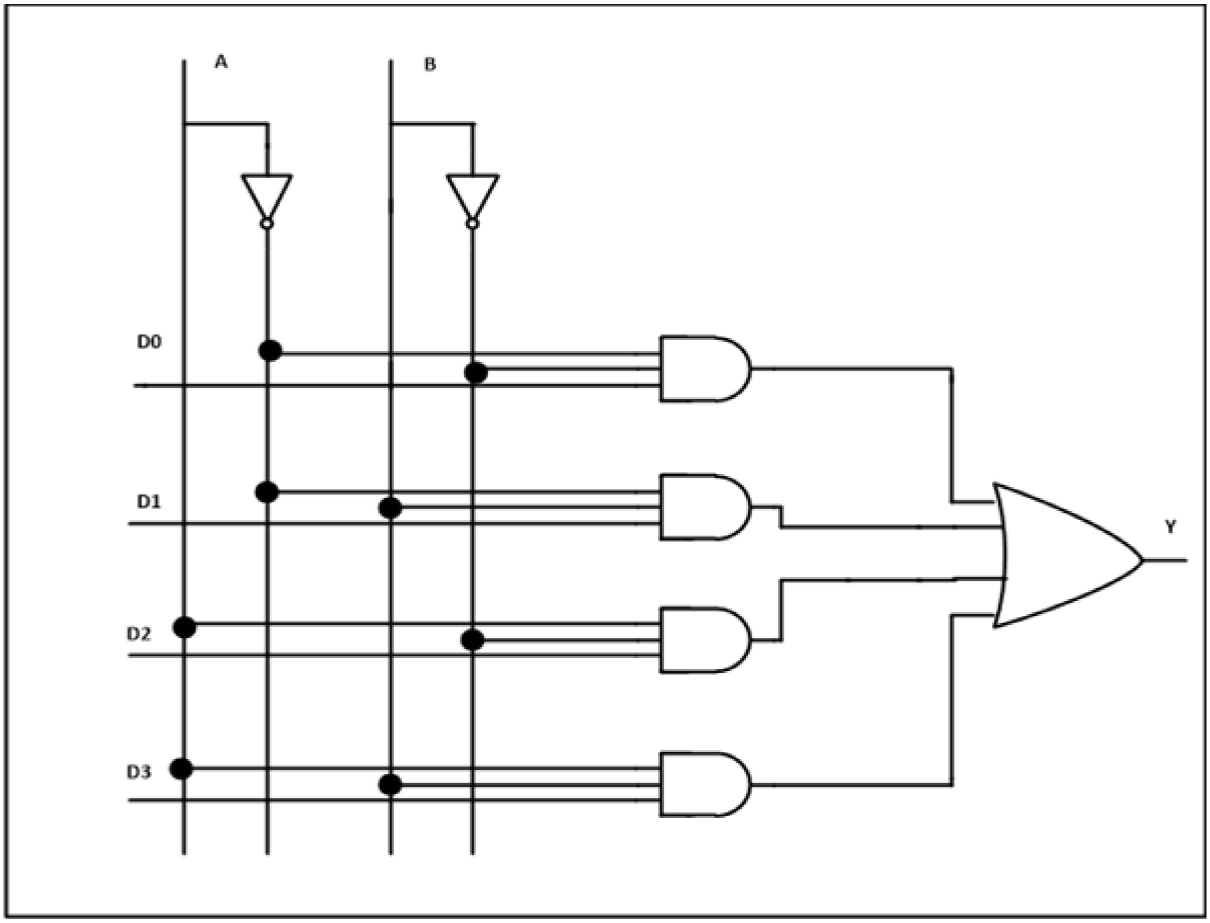


Truth table :-



Select Data Inputs		Output
S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

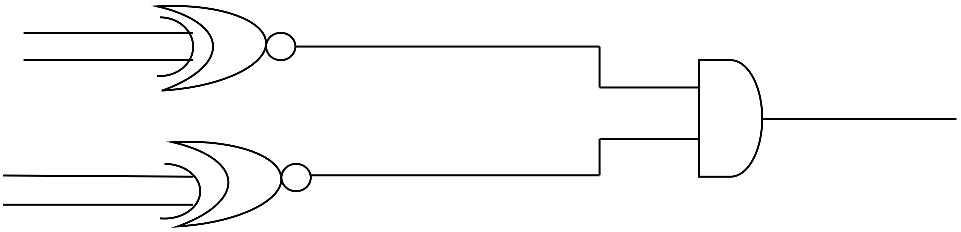
$Y= S_1 S_0 D_0 + S_1 S_0 D_1 + S_1 S_0 D_2 + S_1 S_0 D_3$



2.Design a 2 bit magnitude comparator circuit whose output are A>B ,A=B & A<Bwhere Aand B are each two bit number[2014, 2015,2016,2017]

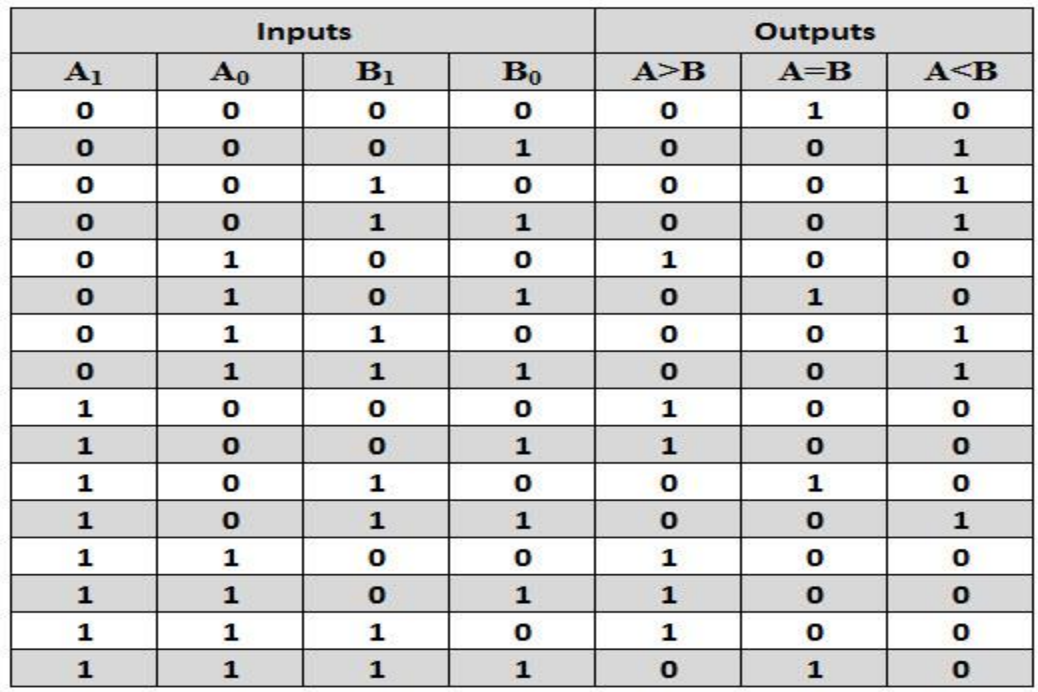
In the evaluation of digital information it is important to compare two binary strings(or binary word say A,B)to determine if they are exactly equal.This is done by using digital comparaors.

Let us consider a 2 bit digital comparator as shown in figure



The inputs are A_1 ,$A_0$and B_1,B_0 outputs are three states :A>B ,A=B and A<B .The logic gates are XNOR .If both the bits are equal i.e 0-0 or 1-1 ,the XNOR outputs are 1.

Truth table :-

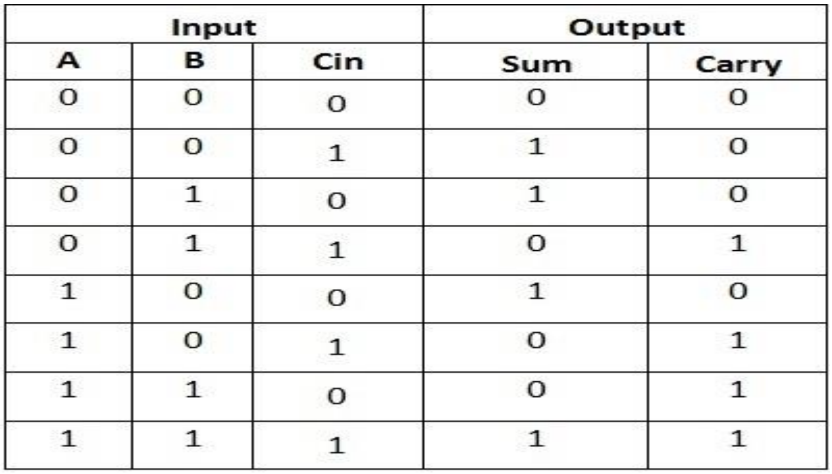


Inputs				Outputs		
A_1	A_0	B_1	B_0	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

3. <u>Design a full adder circuit and implement using NAND gate</u>[2015,2014]

It will perform the addition operation of three binary bits

Truth table



Input			Output	
A	B	Cin	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$S=\overline{X}\,\overline{Y}\,Z+\overline{X}\,Y\,\overline{Z}+X\,\overline{Y}\,\overline{Z}+X\,Y\,Z$

$\overline{X}\,(\overline{Y}\,Z+Y\,Z\,)+X\,(\overline{Y}\,\overline{Z}+Y\,Z)$

$\overline{X}\,(Y\oplus Z)+X\,\overline{(Y\oplus Z)}$

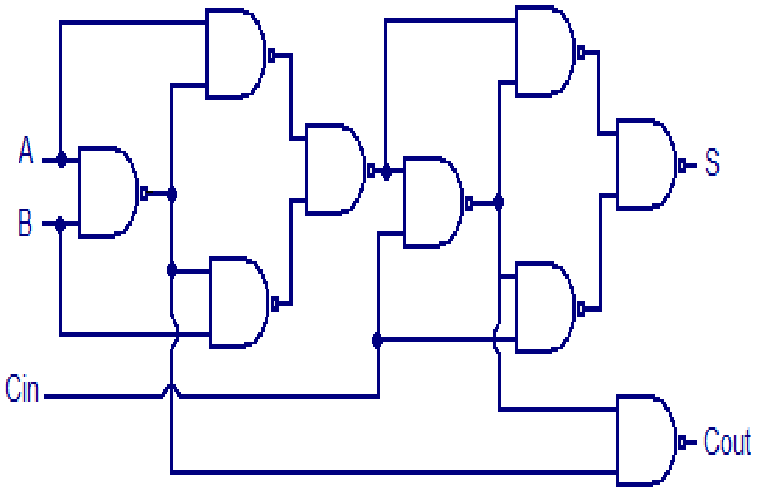
$X\oplus[\,Y\oplus Z]$

$X\oplus Y\oplus Z$

$C=X\,Y\,Z+X\,Y\,Z+X\,Y\,Z+X\,Y\,Z$

$=Z(X\,Y+X\,Y)+X\,Y(Z+Z)$

$=Z(X\oplus Y)+X\,Y$



Chapter 5

2 marks questions

1.<u>What are the difference between CLC & SLC circuit</u>[2013 ,2015]

Same as 5 marks question .

5 marks questions

1. Distinguish between combinational & sequential logic circuit[2014,2016,2017]

Combinational logic	Sequential logic
-In which the output depend on the present input only is known as combinational logic .	-In this case the output depend on present input as well as past output .
-In this case no feedback path is there .	–In this case feedback path is there
--Combinational circuit has no memory	-Sequencial circuit has memory
- -Here we are not using clock pulse.	–In sequencial we use clock pulse.

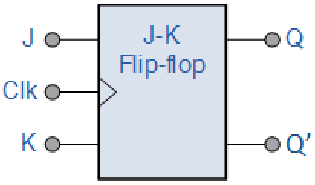
2.Define flipflop and explain clock JK flipflop using NAND gate only.[2016 ,2014]

flipflop

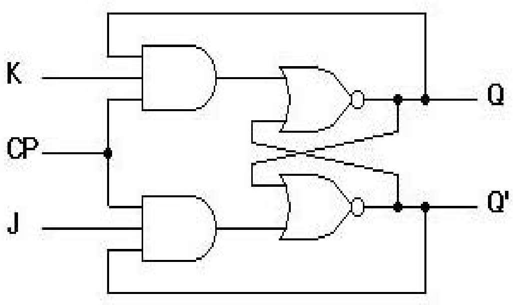
- An electronics, a **flip-flop** or **latch** is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistable multivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs.
- It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems

clocked JK flipflop

- The JK flip-flop is probably the most widely used and is considered the universal flip-flop because it can be used in many ways.

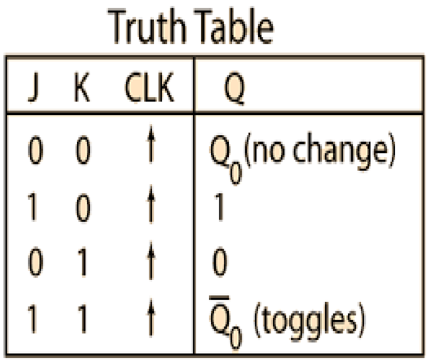


Circuit diagram



The JK flipflop has two inputs J and K .It is the improved version of RS flipflop so that when both inputs 1 then also the output Q and Q are complement to each other .

Truth table :-



Truth Table

J	K	CLK	Q
0	0	↑	Q_0(no change)
1	0	↑	1
0	1	↑	0
1	1	↑	$\overline{Q}_0$ (toggles)

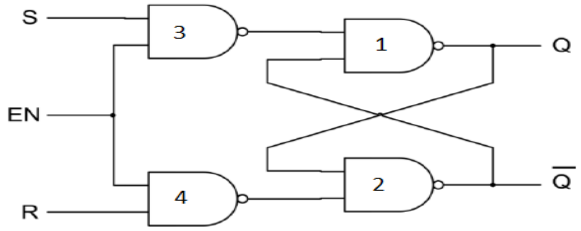
Working Principle :-

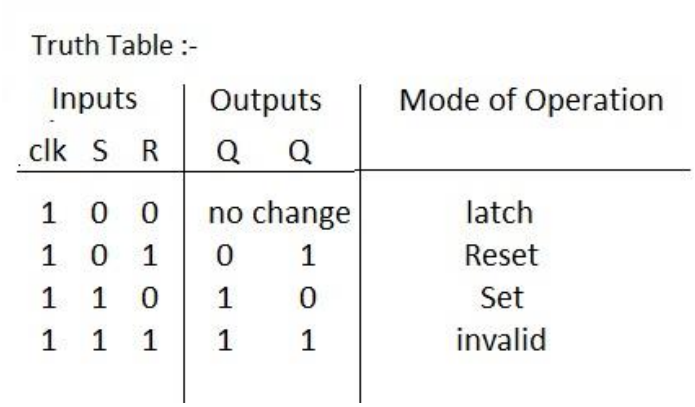
- When J and K both are low ,both AND gates are disolbed and there is no effect of clock pulse and the output remains what it was before the arrived of the pulse
- When J is low and K is high the upper gate is disabled and the flipflop cannot be set and the output Q will be 0 i.e it will reset the flipfliop .
- When J is high and K is low the lower gate will be disabled and the flipflop cannot be reset

When J and K both are high we can set or reset the flipflop depending upon its position at present when J and K both are high what ever may be the output ,it will change to its complement i.e if it is 0 then it change to 1 and if it is 1 then it change to 0 and the condition of flipflop is known as toggle

7 marks questions

1.**Draw the circuit diagram of clock SR flipflop explain it with a functional table**[2016,2017]





Truth Table :-

Inputs			Outputs		Mode of Operation
clk	S	R	Q	Q	
1	0	0	no change		latch
1	0	1	0	1	Reset
1	1	0	1	0	Set
1	1	1	1	1	invalid

In the functional table the explanation is given below :

Let R=S=1 ,Clk=1 ,the output of gates 3 ,4 are both 0 ,making one of the inputs of gate 1 and 2 NAND gates 0.As a result the output Q and Q both will attain high 1 which is in consistent .

For R=0 ,S=1 ,clk =1 ,the output is high i.e Q=1 and Q=0 which is a condition that the flipflop is set

For R=1 ,S=0 ,Clk=1 ,the output is low i.e Q=0 and $\overline{Q}$=1 ,which shows reset condition .For R=0 ,S=0 ,Clk=1 ,the output remains same i.e do not change .

2.Draw and write down the functional table for the conversion of

i) SR to JK flipflop

ii)T to JK flipflop

iii)SR to D flpflop

iv)JK to T flipflop [2014]

ANS ::

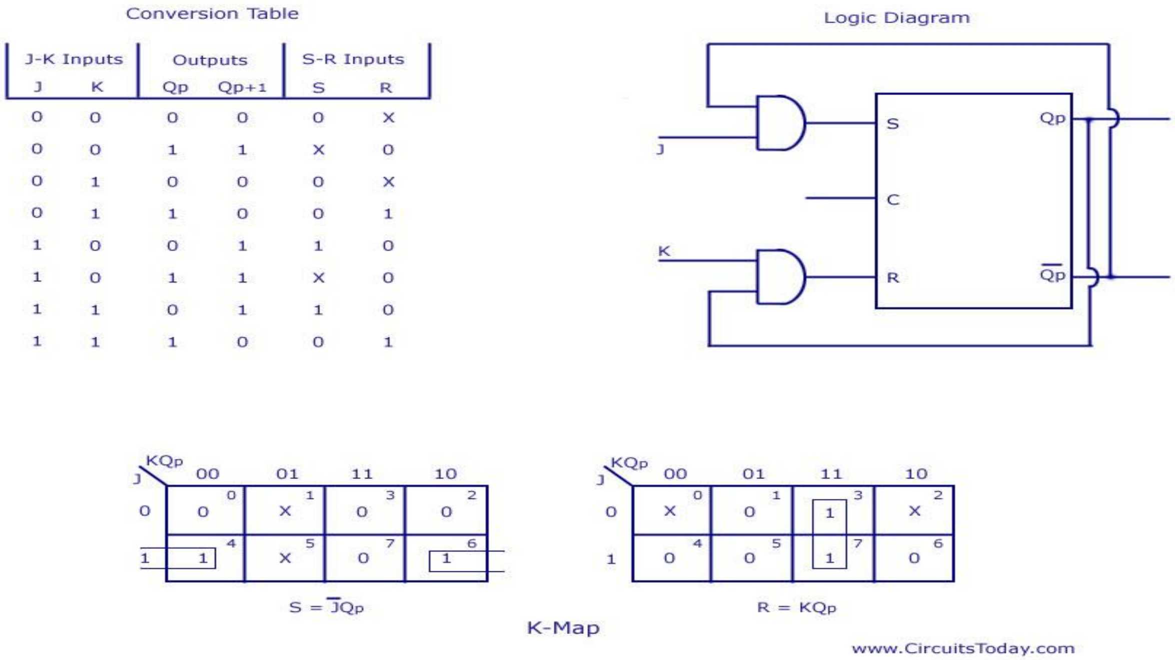
i) SR to JK flipflop

As told earlier, J and K will be given as external inputs to S and R. As shown in the logic diagram below, S and R will be the outputs of the combinational circuit.

The truth tables for the flip flop conversion are given below. The present state is represented by Qp and Qp+1 is the next state to be obtained when the J and K inputs are applied.

For two inputs J and K, there will be eight possible combinations. For each combination of J, K and Qp, the corresponding Qp+1 states are found. Qp+1 simply suggests the future values to be obtained by the JK flip flop after the value of Qp. The table is then completed by writing the values of S and R required to get each Qp+1 from the corresponding Qp. That is, the values of S and R that are required to change the state of the flip flop from Qp to Qp+1 are written.

S-R Flip Flop to J-K Flip Flop



Conversion Table

J-K Inputs		Outputs		S-R Inputs	
J	K	Qp	Qp+1	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

Logic Diagram

J \ KQp	00	01	11	10
0	0	X	0	0
1	1	X	0	1

$S = \overline{J}Qp$

J \ KQp	00	01	11	10
0	X	0	1	X
1	0	0	1	0

$R = KQp$

K-Map

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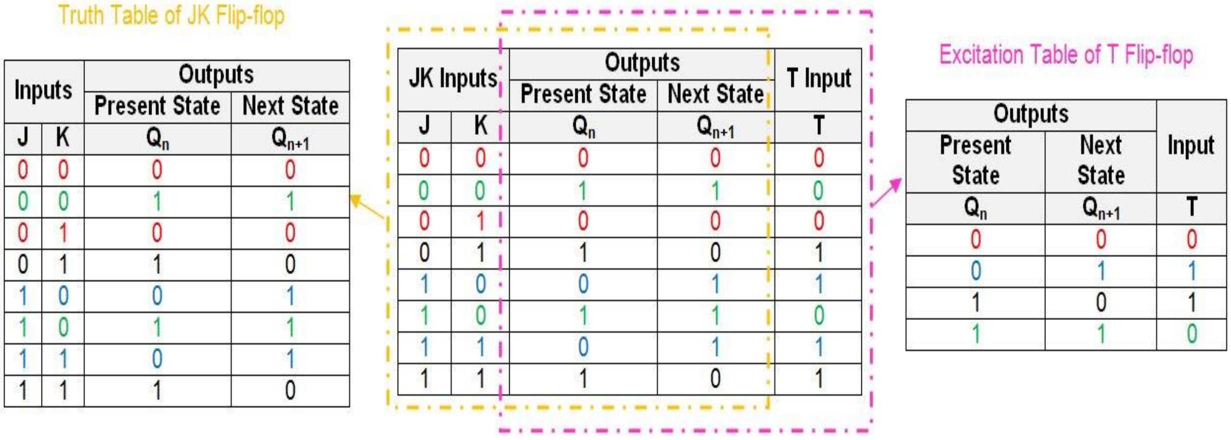
ii)T to JK flipflop :

Conversion of a T to a JK Flip-Flop

We begin with the T-to-JK conversion table (see Figure 5), which combines the information in the JK flip-flop's truth table and the T flip-flop's excitation table.



Truth Table of JK Flip-flop

Inputs		Outputs	
		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

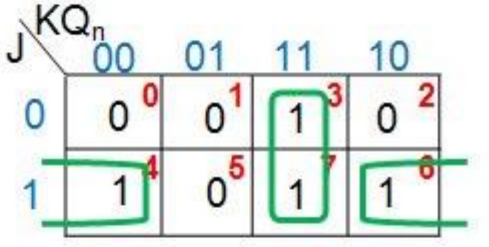
JK Inputs		Outputs		T Input
		Present State	Next State	
J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

Excitation Table of T Flip-flop

Outputs		Input
Present State	Next State	
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T to JK Conversion Table

Next, we need to obtain the simplified Boolean expression for the T input in terms of J, K, and Q_n.



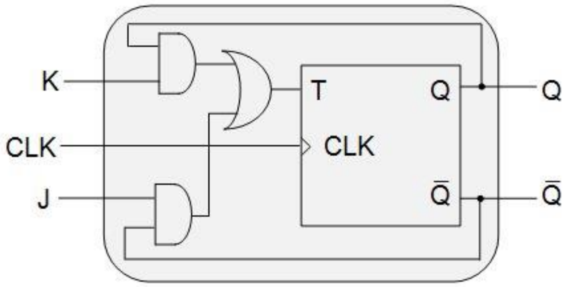
J \ KQ_n	00	01	11	10
0	0^{0}	0^{1}	1^{3}	0^{2}
1	1^{4}	0^{5}	1^{7}	1^{6}

$$T = J\bar{Q}_n + KQ_n$$

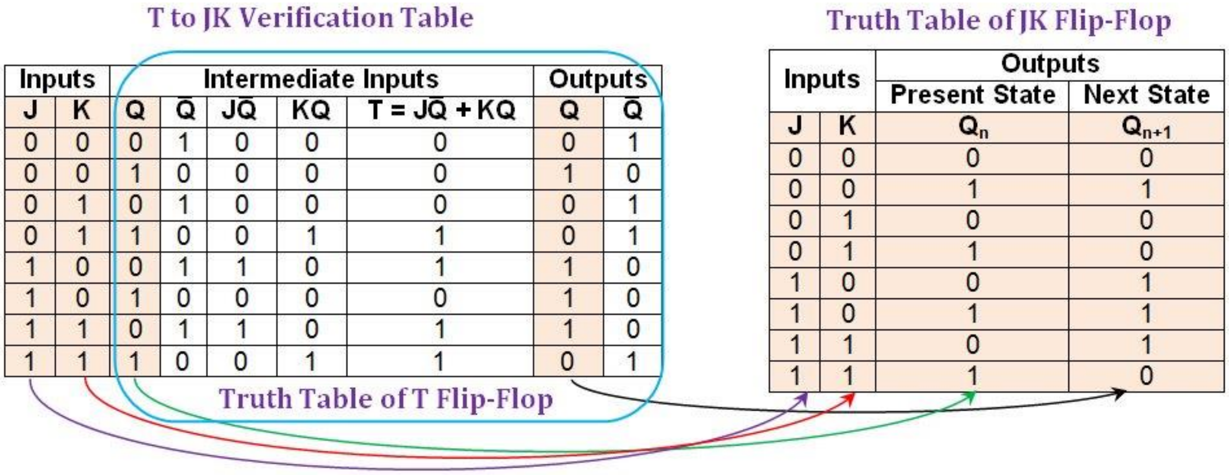
T input as $J\bar{Q}_n + KQ_n$. This means that to convert the T flip-flop into a JK flip-flop, the T input is driven by the output of a two-input OR gate which has as inputs

1. J ANDed with the negation of the present-state Q_n, i.e., $\bar{Q}_n$
2. K ANDed with the present-state, Q_n

Thus, we will need two AND gates and one OR gate, as shown in Figure



The final step is to verify whether the system behaves as we expect it to. This can be done using a T-to-JK verification table, shown in Figure 8. Here we can compare the entries in the verification table to the truth table of the JK flip-flop



T to JK Verification Table

Inputs		Intermediate Inputs					Outputs	
J	K	Q	$\bar{Q}$	$J\bar{Q}$	KQ	$T = J\bar{Q} + KQ$	Q	$\bar{Q}$
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	0	1
0	1	1	0	0	1	1	0	1
1	0	0	1	1	0	1	1	0
1	0	1	0	0	0	0	1	0
1	1	0	1	1	0	1	1	0
1	1	1	0	0	1	1	0	1

Truth Table of T Flip-Flop

Truth Table of JK Flip-Flop

Inputs		Outputs	
		Present State	Next State
J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

The entries in the first, second, third, and eighth columns (shaded in beige) of the T-to-JK verification table agree with those in the truth table of the JK flip-flop. This indicates that the given T flip-flop has become functionally equivalent to the desired JK flip-flop.

iii)SR to D flpflop :

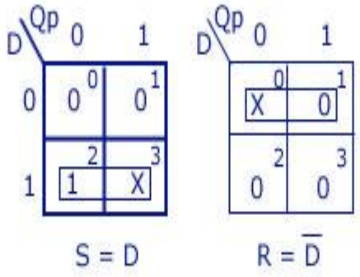
As shown in the figure, S and R are the actual inputs of the flip flop and D is the external input of the flip flop. The four combinations, the logic diagram, conversion table, and the K-map for S and R in terms of D and Qp are shown below.

S-R Flip Flop to D Flip Flop

Conversion Table

D Input	Outputs		S-R Inputs	
	Qp	Qp+1	S	R
0	0	0	0	X
0	1	0	0	1
1	0	1	1	0
1	1	1	X	0

K-maps



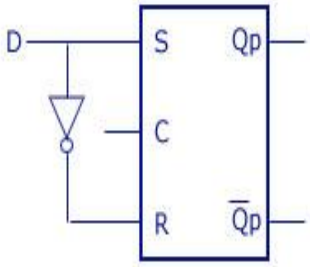
D \ Qp	0	1
0	0	0
1	1	X

S = D

D \ Qp	0	1
0	X	0
1	0	0

$R = \overline{D}$

Logic Diagram



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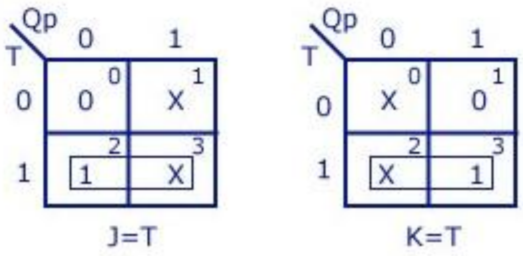
iv)JK to T flipflop :

J and K are the actual inputs of the flip flop and T is taken as the external input for conversion. Four combinations are produced with T and Qp. J and K are expressed in terms of T and Qp. The conversion table, K-maps, and the logic diagram are given below.

Conversion Table

T Input	Outputs		J-K Inputs	
	Qp	Qp+1	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

K-maps

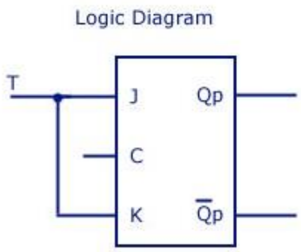


T \ Qp	0	1
0	0	X
1	1	X

J=T

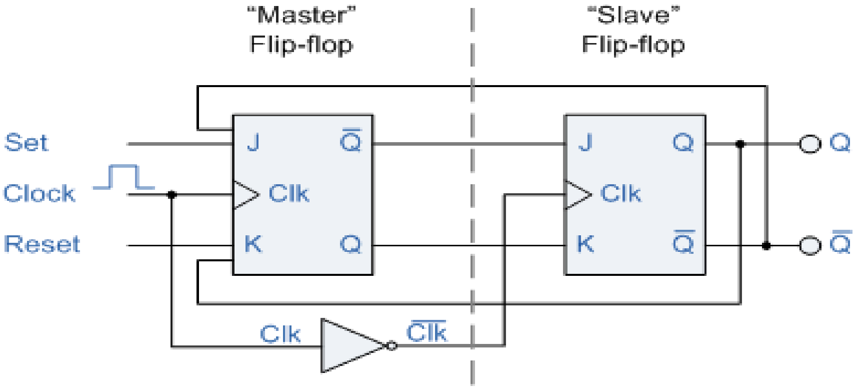
T \ Qp	0	1
0	X	0
1	X	1

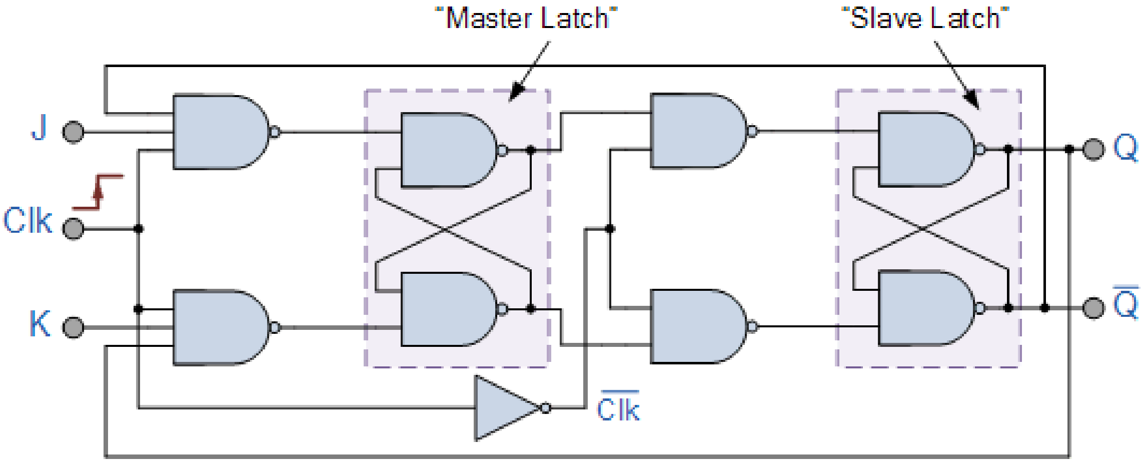
K=T



3.<u>Draw the logic diagram of master slave JK flipflop .Explain it with a functional table</u>[2017]

Master-slave flip flop is designed using two separate flip flops. Out of these, one acts as the master and the other as a slave. The figure of a master-slave J-K flip flop is shown below.

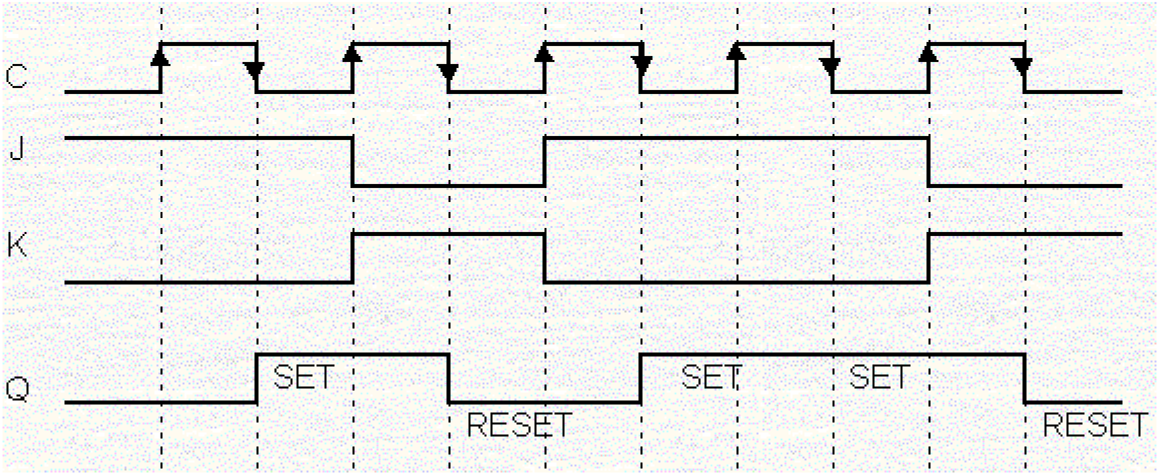




From the above figure you can see that both the J-K flip flops are presented in a series connection. The output of the master J-K flip flop is fed to the input of the slave J-K flip flop. The output of the slave J-K flip flop is given as a feedback to the input of the master J-K flip flop. The clock pulse [Clk] is given to the master J-K flip flop and it is sent through a NOT Gate and thus inverted before passing it to the slave J-K flip flop.

Working

- When Clk=1, the master J-K flip flop gets disabled. The Clk input of the master input will be the opposite of the slave input. So the master flip flop output will be recognized by the slave flip flop only when the Clk value becomes 0. Thus, when the clock pulse males a transition from 1 to 0, the locked outputs of the master flip flop are fed through to the inputs of the slave flip-flop making this flip flop edge or pulse-triggered.
- thus, the circuit accepts the value in the input when the clock is HIGH, and passes the data to the output on the falling-edge of the clock signal. This makes the Master-Slave J-K flip flop a Synchronous device as it only passes data with the timing of the clock signal.



Chapter6

2 marks Questions

1.<u>Define fan in and fan out</u>[2013,2014,2015 ,2016 ,2017]

FAN IN : It is the maximum number of inputs the logic can handle properly.

FAN OUT : The maximum number of load/similar circuits that may be simultaneously driven under worst conditions is termed as fan out of the logic circuit or package .

5 marks questions

<u>1.Explain with sketch the working of 2 input TTL NAND gate</u>[2014]

A TTL NAND gate (schottky) is shown below :

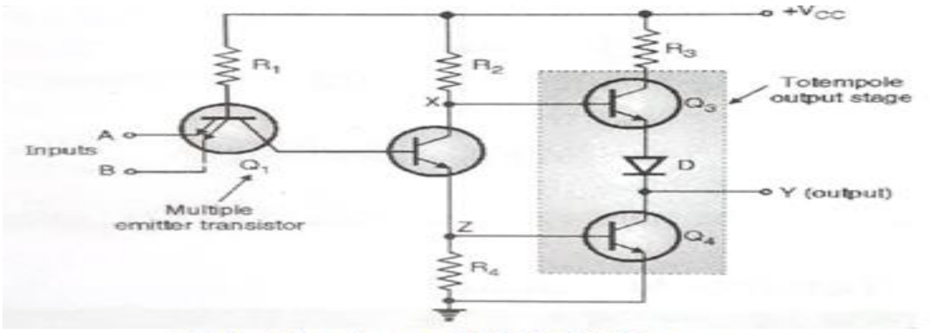


Fig1. Two input TTL NAND gate

It is clear from this figure that the transistor which normally becomes saturated are in this circuit .Schottky clamped transistors and as a result ,the storage delay or saturation delay is virtually eliminated which results in a better switching time .The working of this circuit is more or less such that the transistor being consumed .If e increase the values of resistance of circuit ,the switching action is fast and low power dissipation .There will be minimum propagation delay .When output is high(1),T_0 is off(open) ,T_3 is on(short).When the output is 0(low) ,T_0 is on ,T_3 is off .The current flow from vcc to ground in this section of the circuit ,is minimized .If A=0 ,B=0 or both equal to zero ,output =1 ,the base –emitter diode of T_1 is F.B ,suturing T_1(turning ON)T_2 is off ,T_3 is on .If A=1 ,B=1 ,output=0 ,T_1 is reverse biased ,T_2 is ON.Thus T_4 is on with +ve base voltage ,T_3 is taken off.

Chapter 7

2 marks questions

1.Define modulous of a counter[2014,2017]

Modulous of a counter is defined as equal to the number of states through which the counter progress .The maximum possible number of states is equal to 2^n .Where n=number of flipflops in the counter.

7 marks questions

1.Explain the working of 4 bit ripple counter with truth table and timing diagram [2013,2015 , 2016 ,2017]

The counters in which the output of one flipflop drives the another are called ripple counters or asynchronous counters .

In this case flipflop A has to change state before it can trigger the B flipflop and B has to change for triggering C and so on .

Now we discuss how the counting is carried out by the circuit .

Let us consider that all the flipflop are initially reset to output 0 .Thus the output condition to start with will be DCBA=0000

Now on the arrival of the 1st clock pulse the first flipflop A changes state on occurance of –ve edge of the clock pulse .Hence after the end of first pulse output condition will be DCBA =0001

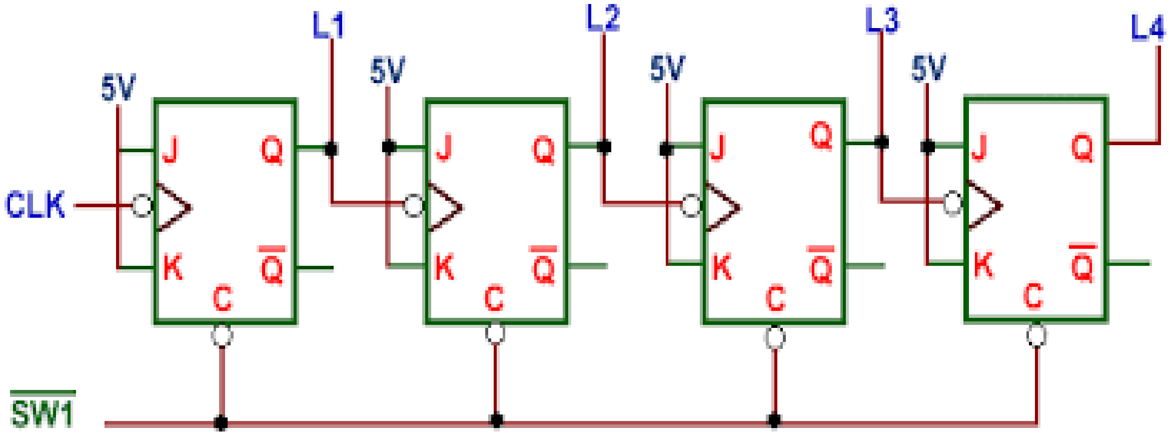
The change of A output from 0 to 1 i.e it is a +ve change and when this +ve change is fed to the clock input of B flipflop ,it cause no change because the change will takeplace only when a –ve edge trigger is applied .

When a 2nd clock pulse arrives at the clock pulse of A flipflop it again change its state i.e it goes from 1 to 0 ,i.e this time at –ve edge so the state of B flipflop is now changes 0 to 1 .This change og 0 to 1 is +ve .So ,after that there is no change now output condition is 0010

Again when we apply clock pulse to A flipflop changes its state 0 to 1 and this is +ve so ,after that there is no change in flipflop output DCBA=0011

In next step DCBA will 0100 ,then 0101 in this way it continue upto 0000.

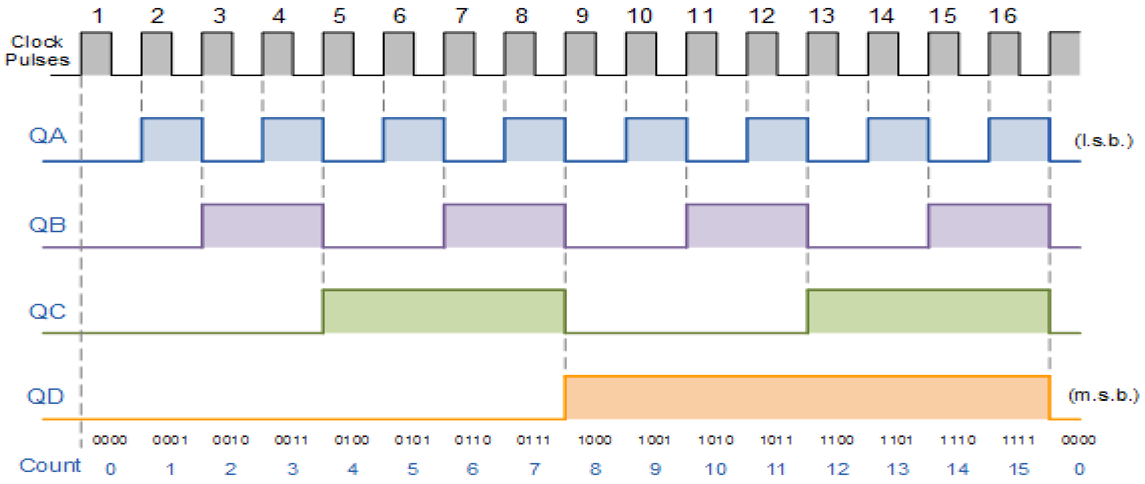
Because here we take 4 flipflop and we require 2^n input pulse i.e 2^4=16 step .



Truth table :-

State	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

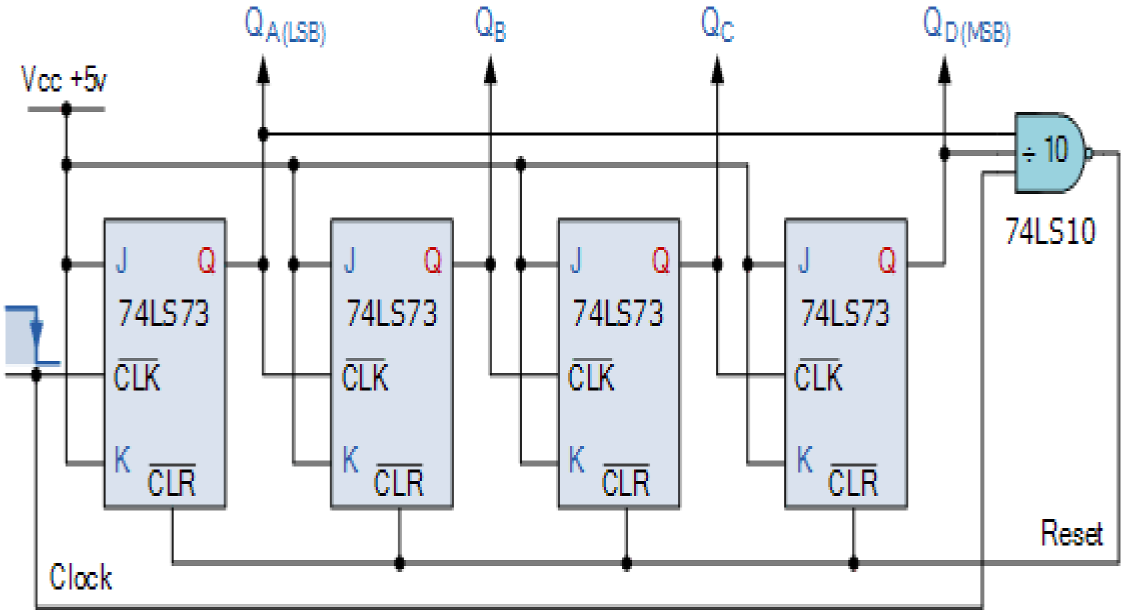
Timing diagram :-



10 marks questions

1. **<u>Explain the working of a Asynchronous type de-cade counter with a neat sketch</u>[2013,2017]**

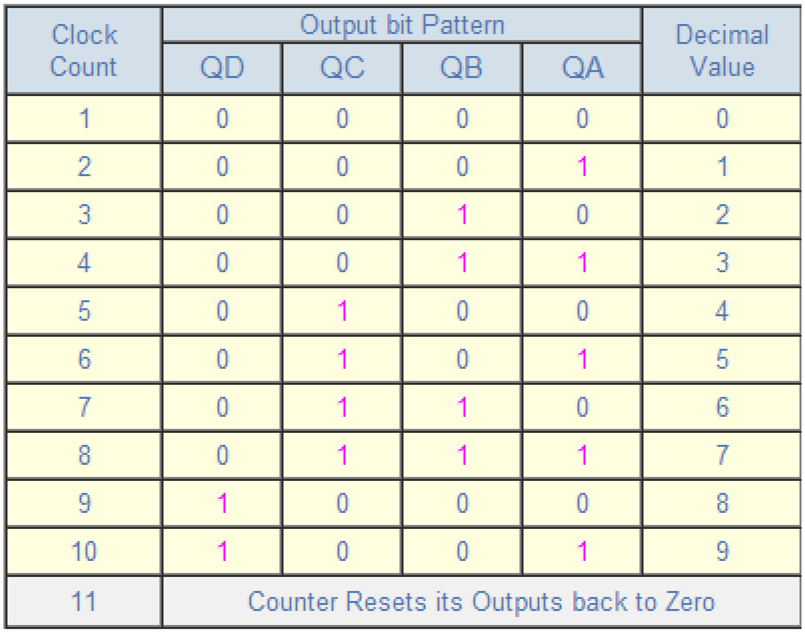
Asynchronous Decade Counter



This type of asynchronous counter counts upwards on each trailing edge of the input clock signal starting from 0000 until it reaches an output 1001 (decimal 9). Both outputs QA and QD are now equal to logic "1". On the application of the next clock pulse, the output from the 74LS10 NAND gate changes state from logic "1" to a logic "0" level.

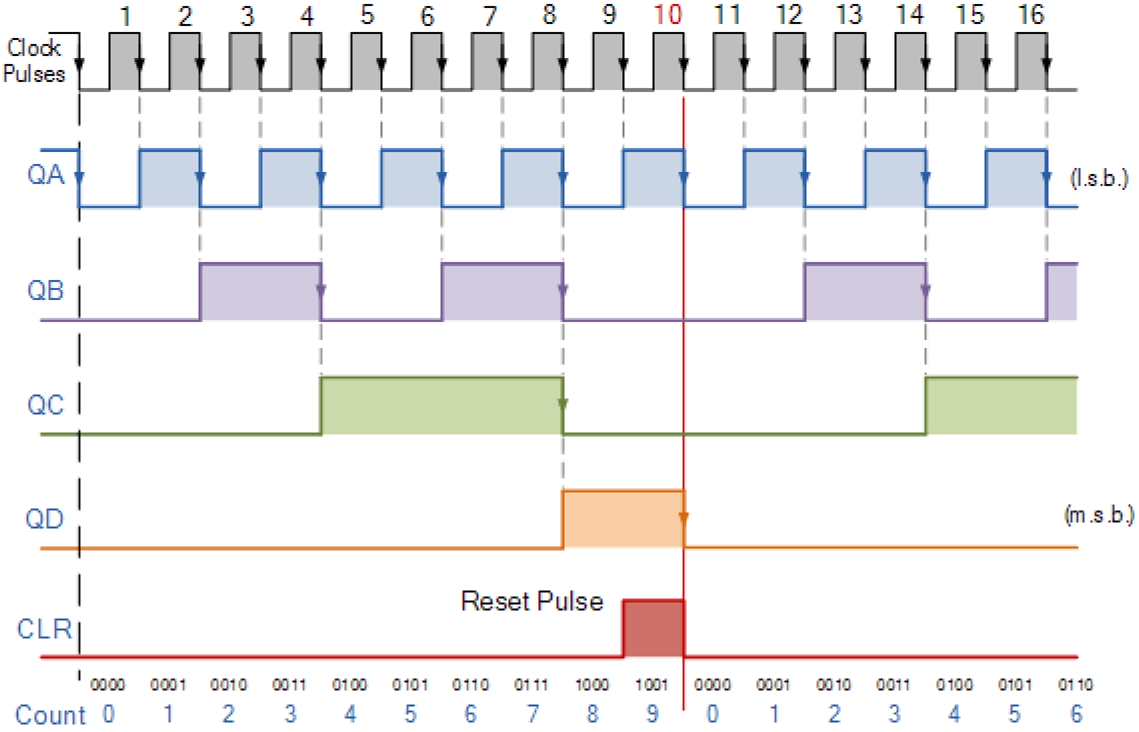
As the output of the NAND gate is connected to the CLEAR (CLR) inputs of all the 74LS73 J-K Flip-flops, this signal causes all of the Q outputs to be reset back to binary 0000 on the count of 10. As outputs QA and QD are now both equal to logic "0" as the flip-flop's have just been reset, the output of the NAND gate returns back to a logic level "1" and the counter restarts again from 0000. We now have a decade or Modulo-10 up-counter.

Decade Counter Truth Table



Clock Count	Output bit Pattern				Decimal Value
	QD	QC	QB	QA	
1	0	0	0	0	0
2	0	0	0	1	1
3	0	0	1	0	2
4	0	0	1	1	3
5	0	1	0	0	4
6	0	1	0	1	5
7	0	1	1	0	6
8	0	1	1	1	7
9	1	0	0	0	8
10	1	0	0	1	9
11	Counter Resets its Outputs back to Zero				

Decade Counter Timing Diagram



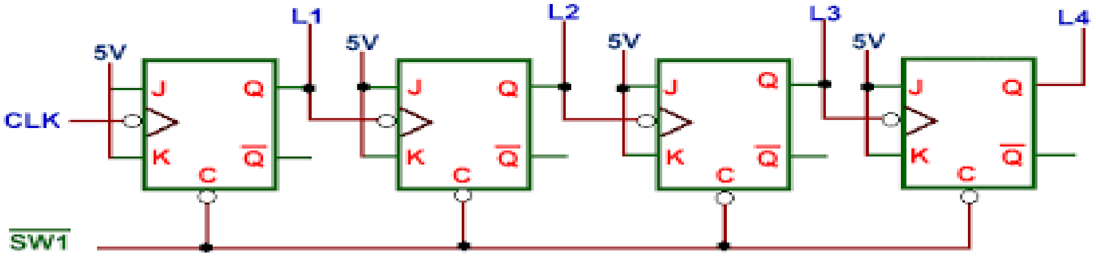
Chapter 8

6 marks questions

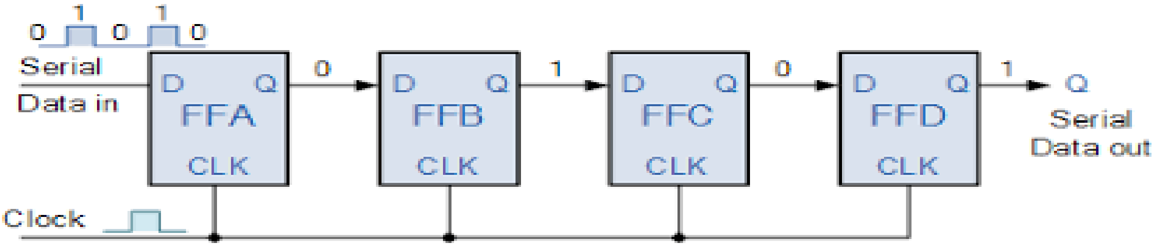
1. With a neat diagram explain the operation of PISO register[2014]

PISO (parallel in serial out):

In such resisters where we have parallel input ,the data bits are entered simultaneously into their respective stages on parallel lines & not on a bit by bit basic on one line as well the case with serial in registers .Serial outputs of these resisters are taken out the same way as we explained for (SISO).After the data bits are properly stored once in the resister the data bits are taken out one by one as was the case with SISO resister .



2.With neat sketch explain the working of 4 bit SISO register with a neat diagram and timing diagram[2013]



In serial in serial out shift register the binary data is accepted serially i.e one bit at a time is accepted on a line .The stored information is also produced at the output in serial form

As this is a 4 bit register its storage capacity will be 4 bit & will require 4 flipflops to construct it .

Let us consider that the number to be entered be 1010 .Intially counter is in reset on all 0 state .The data line feeds the data word one by one bit starting from the rightmost bit .

First 0 is put on the data input line .This makes S_1 =0 & R_1=1 as the complement of S_1 is fed as R_1 on the occurrence of first pulse under (S_1 =0 & R_1 =1)the 1st flipflop resets & 0 is stored now next bit of data word which is a 1 input on input dataline which makes S_1 =1 & R_1=0 and forces first flipflop to change its state from 0 to 1 on the occurrence of 2nd pulse .Flipflop doesnot change its state .

Now the 3 rd bit of data word 0 is put on data input line .This makes S_1 =0 & R_1=1 for first flipflops and on the occurance of 3rd clock pulse the output state of 1st flipflop is changed to 0 from 1 while 2nd flipflop changes from 0 to 1 .The thired flipflop does not change its state .

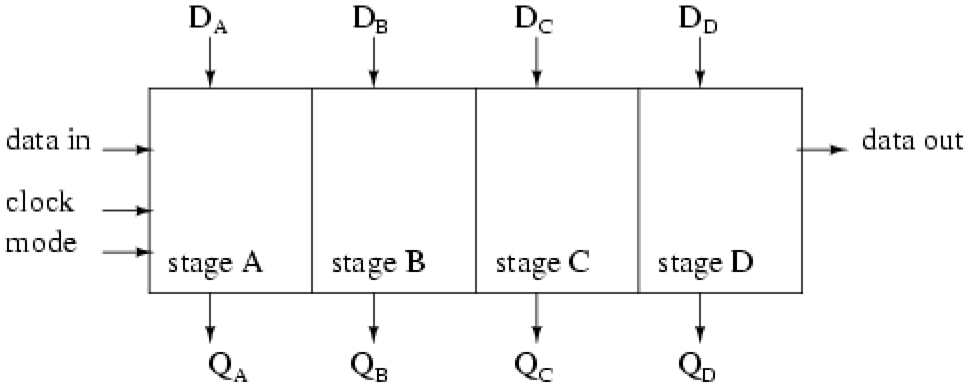
Now we put 4th bit of data 1 on the data input line which makes S_1 =1 & R_1=0 .Hence when 4th clock pulse occurs flipflop 1 ,2 ,3 change their state while 4th flipflop doesnot change its output state forcing Q_1 =1 ,Q_2 =0 ,Q_3=1 ,Q_4=0 ,So the data word 1010 is shifted into the resister .

7 marks questions

1.With neat sketch explain the working of PIPO and SIPO registor[2016 ,2017]

PIPO :(parallel in parallel out)

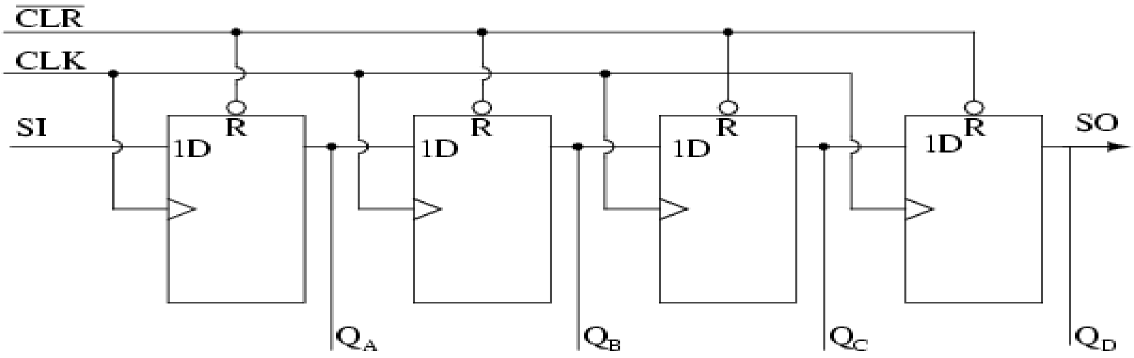
Here data is given simultaneously to all flipflops and also data is collected from all the flipflops simultaneously .



Parallel-in, parallel-out shift register with 4-stages

SIPO(Serial in parallel out)

It is the shift register that accepts data seriously and gives data parallel .Here output is taken from all flipflop simultaneously.



Serial-in/ Parallel out shift register details

Chapter 9

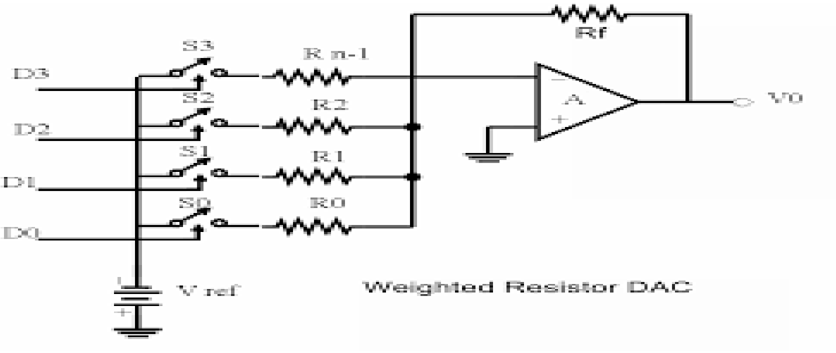
7 marks questions

1. **Define the term offset voltage of D/A converter .Explain the working of weighted resistor type DAC converter with a neat block diagram[.2014]**

In a D/A converter ,off set voltage is the analog output voltage produced according to the binary word .For example if the binary word is 0010 the voltage is 2v .

The most simple and straight forward method of converting digital to analog involves the use of a resistor network .The resistors used in these networks weigh the current passing through them which are then summed up .

A basic network for an N-bit is shown in figure(a) the resister values are weighted inversely with their current values .(for example if we want the current should be half of the fixed resister)We take the resistance to be two times of R i.e 2R if it is to be ¼ we take resistance to be 4R and so on)In this figure the resister R ,2R ,4R ,8R………2^{N-1}R are weighted resistors which can be connected through the electronic switches .



Weighted Resistor DAC

In a 4 bit resister network as shown in fig.(b) when the switch S_3 connects the resister R to the +5v line (V_0) and all other resister are grounded .The current through R will be $V_0/R(=5/R)$.If the resister R is of 1kΩ the current will be 5mAQ .Now if S_2 connects 2R (=2kΩ)+5v keeping other resisters grounded ,the current will be $V_0/R=2.5$ mA ,which is one-half of the previous current value .Similarly when S_1 and S_0 are connected the current through other resisters wil be V/4R and V/8R or 1.25 and 0.625 respectively .This shows that the current in the resisters is reduced in proportion to their resistance values ,the currents will also be reduced in binary proportions .When these currents are summed up at common terminal C then the total current will be given by

$I_t=I_{N-1}+I_{N-2}\ldots\ldots I_2+I_!+I_0$

When $I_{N-1}=V_{N-1}/R$,$I_{N-2}=V_{N-2}/2R\ldots..I_0=V_0/2^{N-1}R$

Hence $V_0(A_3/R+A_2/2R+A_1/4R+A_0/8R)$

$V_C(1/R+1/2R+1/4R+1/8R)$

Or $V_C(8A_3+4A_2+2A1+A_0)V_0/15\ldots\ldots\ldots\ldots\ldots.(i)$

The coefficient A_3 ,A_2 ,A_1 and A aew 1 when the switch connects a resisters to V_0 otherwise it is a 0 . If we consider the V_0=5V and $A_3=1$,$A_2=A_1=A_0=0$ that is for 1000

$V_C=8/15\times4=8/3$

Similarly ,0001,will be=1/15×5

0010 ,will be =2/15×5

0100 ,will be 4/15×5 etc

Hence the output voltage from the binary weighted resistors network are proportional to the binary input .The general form of equation (i) will be

$V_C(2^{N-1}\ A_{N-1} +2^{N-1}\ A_{N-2} +\ldots 2^3 A_3\ +2^2\ A_2\ +2^1\ A_1\ +2^0\ A0)V_0/2^N\ -1$

The number of resistor to be used in the resistor network is equal to the number of bits .A N bit resistor will require N resistors .In case of a 8 bit resistor network the LSB resistor will have a resistance of 128 times bigger in value than the MSB resistor.

A basic type of resistor network D/A converter is shown in fig. For a 4 bit D/A converter and uses 4 inputs .The resistances used has the values the represent the binary weights of the input bits of the digital code .The switch symbols represent transistor switches for inputting each of the 4 bits .R_F is the feedback resistance ,The operational amplifier offers a very high impedance load to the resistor network ,and its inverting inputs looks like virtual ground .As a result the current through the feedback resistance is sum of the input current and the output and is proportional to the current through the R_F ,as practically all the current is through R_F ,and into the output of the operational amplifier .The inverting input to the OP-AMP is at 0v.

The high binary weighted input or the MSB input (2^3) corresponds to lowest value resistor .Other resistors are multiplies of R i.e *R ,4R and 2R ,corresponds to the binary weights 2^2 2^1 2^0 respectively .If V_R is the reference voltage ,then the current in the feedback resistor when a state 1000 is at digital input will be given by $I=V_R/R$

(as no current passes through resistors 2R ,4R and 8R)

If the digital input is 1111 then the current through the feedback resistance will be

$I=V_R[1/R+1/2R+1/4R+1/8R]$

$=V_R/R[1+1/2+1/4+1/8]=1.875V_R/R$

The output voltage V_0 is given by

$V_0=-(-V_R)(\frac{R_F}{R}A_{N-1}+\frac{R_F}{2^1R}A_{N-2}+\frac{R_F}{2^2R}A_{N-3}+\cdots\ldots\frac{R_F}{2^{N-1}R}A_0)$

Which is of the form of equation .Hence the output voltage for fig. (b) is given by

$V_{0UT}=\ \frac{R_F}{2^{N-1}R}(2^{N-1}V_{N-1}+2^{N-2}V_{N-2}+\ldots\ldots+2^1V_1+2^0V_0)$

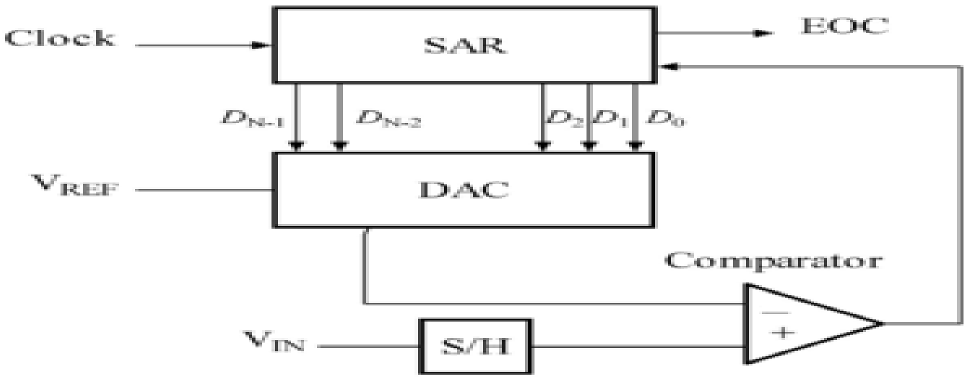
The output swing is in one direction only I.e ,it is unipolar .For converting the data into bipolar format as in case of sign –magnitude ,1’s complement or 2’s complement format ,then V_0 = 0 and so V_0 is used to orr set the output swing .Such an arrangement is shown in fig .(c) .The off-set voltage produced in this circuit is $-\frac{R_F}{R_{OFF}}\,.V_{OFF}$

Chapter 10

5 marks questions

1. Explain Ramp type with a neat circuit diagram[2015]

This method of analog to digital conversion is known as digital ramp or counter method .This is the least expensive and slowest method but it is an ideal method .

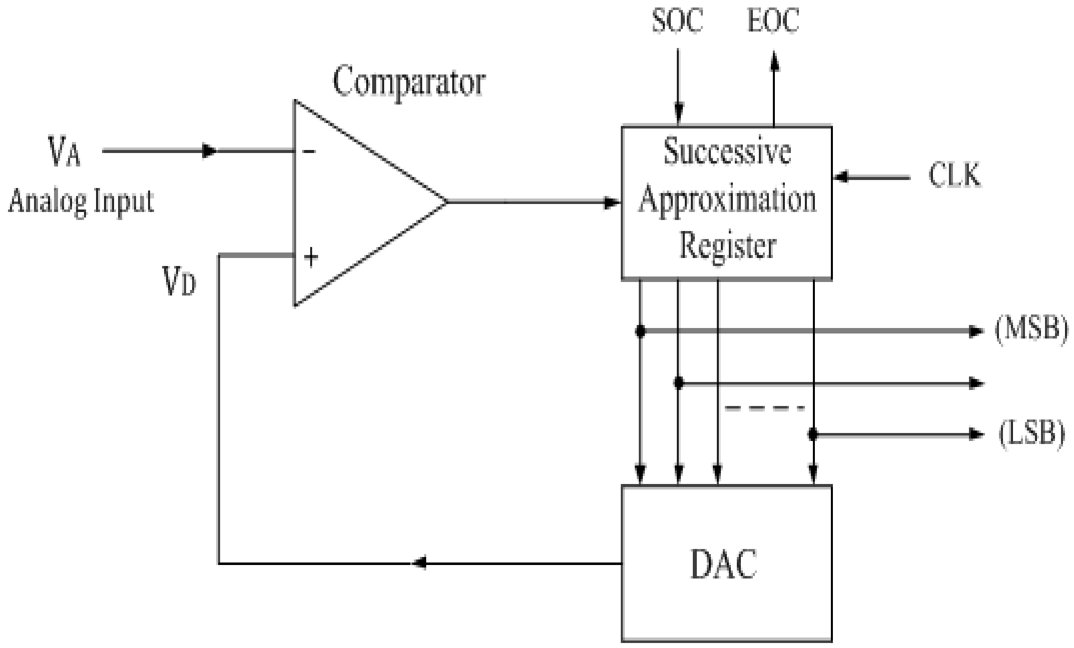


Here analog input is converted into digital and given to comparator,then convert signal is send to control circuit .The control circuit resets the counter and then supplies clock pulse to the counter .The binary output from the counter is given to D/A converter which converts the analog input to digital voltage ,and this sends to comparator for comparing the D/.A converter output with the analog input .

10 marks questions

1. Explain the working of a successive approximation type A/D converter[2013]

There A/D converters have very small conversion time i.e of few milli seconds . The conversion time is fixed and does not depend upon the value of analog input .A logic diagram for a successive approximation A/D coverter is shown in figure .



It consists of a successive approximation register ,a comparator and a D/A converter .The basic working of this converter can be understood as follows .The bits of the D/A converter was enabled one bye one starting from the MSB one at a time .As each bit is enabled ,the comparator produces no output indicating wheather the analog input voltage is greater or less than the output of the D/A converter .If the D/A converter output is greater than the analog input ,the bit of this is less than the analog input ,the bit is retained in the resister .The system starts with MSB first ,then next significant bit and so on .After all the bits of the D/A converter have been examined in this way the conversion cycle is completed .This method is very fast and in some units conversion takes place in less than 250 ns/bit .

The comparator compares the output of D/A to the analog input and derives the successive approximation register .A SAR is special purpose register designed for this purpose using MSI logic .

Let us consider a 4 bit converter and the analog level is full scale analog level .On receiving convert signal the conversion starts and first MSB is made a 1 and the out put of D/A converter is compared with the analog input

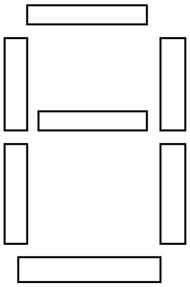
Chapter11

5 marks questions

1.Explain the operation of segment display[2016 ,2014]

In digital systems ,the output or the result is displayed as digit on a display unit .These number are displayed on a pocket calculator ,digital voltmeters ,digital watches and many other devices by a code known as seven segment display code .

The 7 segments are S_0 ,S_1 ,S_2 , S_3 , S_4 , S_5 and S_6



Truth table :-

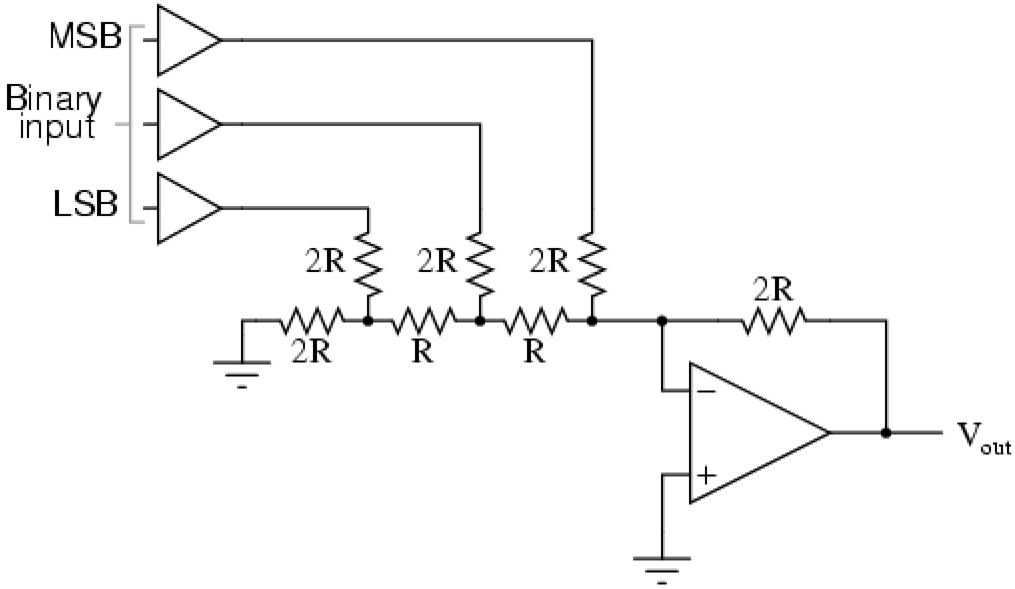
Input				Decimal equivalent	Seven segment						
A	B	C	D		S_6	S_5	S_4	S_3	S_2	S_1	S_0
0	0	0	0	0	0	1	1	1	1	1	1
0	0	0	1	1	0	0	0	0	1	1	0
0	0	1	0	2	1	0	1	1	0	1	1
0	0	1	1	3	1	0	0	1	1	1	1
0	1	0	0	4	1	1	0	0	1	1	0
0	1	0	1	5	1	1	0	1	1	0	1
0	1	1	0	6	1	1	1	1	1	0	1
0	1	1	1	7	0	0	0	0	1	1	1
1	0	0	0	8	1	1	1	1	1	1	1
1	0	0	1	9	1	1	0	1	1	1	1

For this a 7447 IC is essential .This IC is a decoder which converts the BCD input to its corresponding 7 segment code .This code is used to light up the corresponding LED in the display so that the BCD numbers is displayed in decimal .

2.Explain R-2R lader type DAC with a neat diagram[2015]

Let us consider ladder network R/2R network for DAC as shown in the given figure .

R/2R "ladder" DAC



When switch S_1 is switched on to r_{ef} voltage and S_2 ,S_3 and S_4 are ground .The network becomes as shown in figure below .Now looking down from fig.

A the resistance is 2R ,looking up from fig .A is 2R .Hence the total resistance seen by fig. A is 3R .Looking down and left and D we have 2 resistance in parallel of 2R which means we have a resistance of R only ,When looking down from D .Now we have resistance (R)between C and D so looking at C we have resistance of 2 R .In this way at point B .A the resistance are calculated as

Total resistance seen by fig. is 3 R

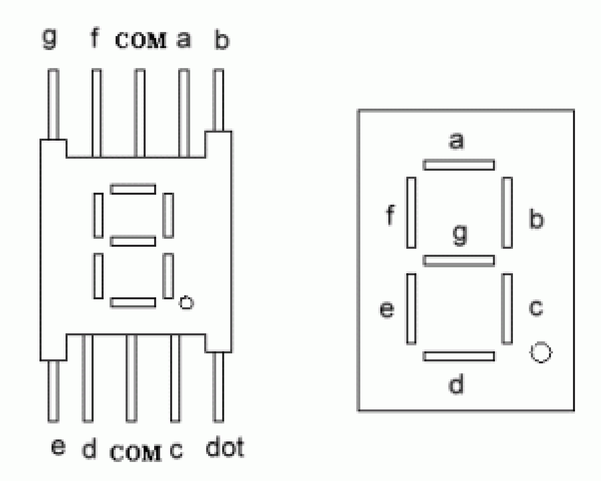
Total current (I)=VR/3R

7 marks questions

1. Explain LED driver using ic 7447 decoder [2015]

The Light Emitting Diode (LED), finds its place in many applications in this modern electronic fields. One of them is the Seven Segment Display. Seven-segment displays contains the arrangement of the LEDs in “Eight” (8) passion, and a Dot (.) with a common electrode, lead (Anode or Cathode). The purpose of arranging it in that passion is that we can make any number out of that by switching ON and OFF the particular LED’s. Here is the block diagram of the Seven Segment LED arrangement.

Pin configuration of a seven segment display:



Seven-Segment Display

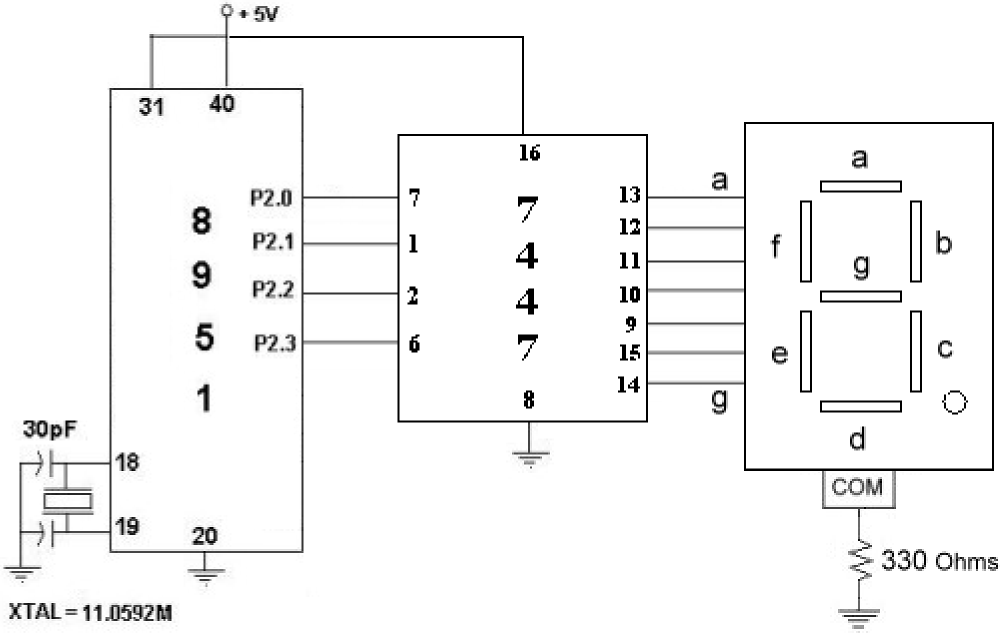
LED’s are basically of two types:

1. Common Cathode (CC)
   All the 8 anode legs uses only one cathode, which is common.
2. Common Anode (CA)
   The common leg for all the cathode is of Anode type.

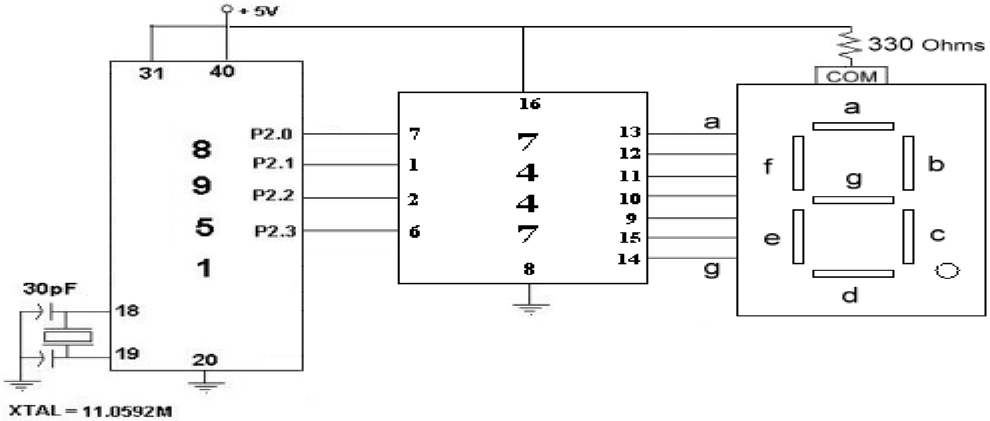
Using 7447 decoder:

The IC7447 is a BCD to 7-segment pattern converter. This setup is the advanced form of the <previous> setup where we entered the patterns manually to display the desired character. Here in this case, the IC7447 takes the Binary Coded Decimal (BCD) as the input and outputs the relevant 7 segment code. We connect first four pins of the microcontroller Port 2 to the 7447 and the Output 8 pins of 7447 to the 8 legs of the LED as shown in the figure. Te circuit diagrams are shown below, the first figure is interfacing the CA LED where as the second is of CC LED. The number required to display is sent as the lower nibble of the

Port 2 of the Microcontroller. The 7447 converts the four input bits (BCD) to their corresponding 7-segment codes. The outputs of the 7447 are connected to the 7-segment display.



(circuit diagram for common anode)



(circuit diagram for common cathode)